Method to Reduce Quantization Error in Direct Interface Circuits for Resistive Sensors

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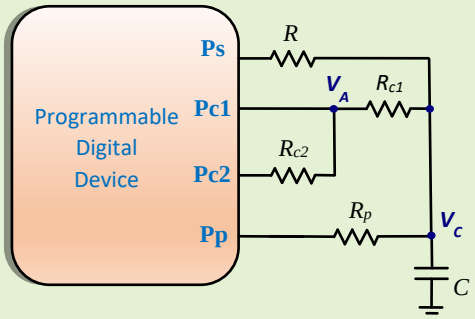
***Abstract*— Reading resistive sensors and converting their information to digital values is a matter of great interest in practical applications. Direct Interface Circuits (DICs) perform this task efficiently through a resistance-to-time-to-digital conversion. The main benefit of this type of circuit is the simplicity of its design and the accuracy of the results. However, one of its drawbacks is that quantization errors in the measurements seriously compromise accuracy if the information is not converted using a high-frequency clock or with high capacitor values. To avoid this situation, this article presents a new type of DIC with the same passive elements as a classic DIC, but which uses a high value resistor in the final instant of the resistance-to-time conversion. The circuit has been implemented using a commercial FPGA with the capture module operating at different clock frequencies. The results show that relative errors in measuring resistors of up to 33 Ω decrease to 1.56% when operating with a 12.5 MHz timer.**



***Index Terms*— Direct interface circuits, calibration methods, error analysis, quantization error, resistive sensor, interface sensor, time-based measurement.**

I. Introduction

DIRECT Interface Circuits (DICs) are a family of circuits designed to read the electrical properties of a sensor, transforming this information into a digital measurement. This type of circuit was initially proposed, practically at the same time, by Sherman and Webjörn [1], [2]. Performance of these circuits is similar to that obtained by a conditioning circuit and an analog-to-digital converter [3], but using minimal hardware. DICs perform sensor reading using a programmable digital device (PDD), which obtains the digital value of the measurement with at least some passive components. For a circuit to be considered a DIC, some of the sensor terminals must be connected to the PDD, either directly or through passive elements. Some DICs can be designed with additional active devices, which are generally simple and few in number (transistors, triggers, etc. [4]). Other DICs may use more complex elements, such as amplifiers or even analog-to-digital converters, in which case these elements must be integrated within the PDDs themselves [3], [5]. DICs allow the use of microcontrollers [6]–[11] or a field-programmable gate array (FPGA) [12]–[15] which shows the versatility of the method. Moreover, using PDDs allows a DIC to work as a smart sensor, since the converter data can be processed by the PDD itself, reducing any central processing unit load.

Another important common feature in all DICs is that the digital value of a readout is obtained by measuring different times, some of which are used for calibration purposes. All these times are digitally processed in order to obtain the sensor's electrical parameters. A DIC therefore performs a sensor magnitude-to-time-to-digital conversion [16].

There are DICs for reading different kinds of sensors: resistive [4], [9], [17] differential resistive [18], resistive arrays [12], [15], capacitive [19]–[23], inductive [10],[24]–[26] differential inductive [11], [27], and even DICs designed to simultaneously measure any of the aforementioned sensors [5]. The DICs for each type of sensor are usually different and have their own benefits and drawbacks. Of all types of DICs, those designed to read resistive sensors have been the most studied in the literature. Issues such as accuracy, uncertainty, resolution [8], [10], [26], [28], [29] power consumption [7], calibration points [30] and response to dynamic signals [31] have been all extensively studied.

From analysis of this literature, it can be deduced that resistive DICs present limitations on the reading of very high or very low resistances. One of the biggest problems when measuring high resistances is the excessive time required for estimating the resistance value, $T_E(R)$. This time, in the case of DICs for resistive sensors, is the sum of all the times necessary to charge and discharge a capacitor and increases with the value of the resistor to be measured, which, in certain applications, limits the resistances that can be measured. However, a calibration method has recently been proposed that considerably reduces $T_E(R)$, in exchange for a slight increase in estimation error [14].

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As for low resistances, one of the main problems related to their reading is the uncertainty in their value, caused by the quantization process when converting the measure to a digital value. Uncertainty of quantization occurs since measurement of time intervals in a PDD must be performed in an integer number obtained by a timer. Quantization uncertainty is therefore constant for the entire range of resistances, and, in the case of high resistances (at least several kiloohms), its value is considerably lower than the measurement uncertainty caused by trigger voltage variations in the input pin of the PDD as a result of electrical noise in the circuit. However, this latter uncertainty decreases in line with R, meaning quantization uncertainty increases its relative importance for low resistance values. In consequence, quantization uncertainty is the main source of inaccuracy in measurements for resistances below a few hundred ohms [16]. Given these facts, DICs present relative errors in the resistance estimation that are a function of the resistance value itself (among other factors) and are generally low for medium/high resistances and have high peaks for low resistances. The result is that resistive DICs do not usually measure resistances below a few hundred ohms. However, there are interesting practical applications in which resistive sensors have resistivities below these values, such as, among many others, sensors based on the hot-wire method [32] or on detecting certain types of gases.

Quantization uncertainty can be reduced by increasing the value of the capacitor that is normally used in resistive DICs, or by increasing the clock frequency of the PDD. However, these solutions have the drawback of increasing the power consumed by the system [7] or $T_E(R)$, meaning they are not attractive solutions. In [33], the problem is addressed differently. This paper proposes applying the basics of mechanical Vernier calipers to a DIC. In this case, the procedure is based on several mathematical approaches and requires additional components and capacitor charge and discharge cycles. Even so, the method can increase resolution 10 times in a 1 kΩ resistor. However, errors in measurements are not available.

To avoid problems arising from the use of an approximate method and additional components or measurement cycles, this article presents a new type of resistive DIC that, without additional cycles and based on an exact mathematical solution, reduces uncertainties due to quantization without significantly modifying those caused by electrical noise when low resistances are measured. This new DIC, and its simplicity of design, can benefit applications that did not hitherto use this methodology.

The structure of the paper is as follows. Section II shows the operating principles of different types of DICs and their fundamental characteristics. Section III presents the new DIC proposal. Section IV presents the materials and methods used in evaluating the new proposal. Section V shows the experimental results. Finally, the conclusions are presented in Section VI.

II. Background Operating Principle

Two types of resistive DICs are the most cited in the literature. The first one is shown in Fig. 1 (a) and is known as the Two-Point Calibration Method, TPCM. The circuit consists of a PDD, a resistor, R_p, to charge the capacitor C to the supply voltage of the PDD, V_{DD}, two calibration resistors of known value, R_{c1} and R_{c2} ($R_{c1} < R_{c2}$), and the resistive sensor to be measured, R. The function of R_p is to limit the load current, and may be omitted depending on the PDD used (although it is stated in the literature that its use can reduce the influence of power-supply noise on circuit performance [34]). The operation principle is simple: three charge cycles of the capacitor are performed through R_p and, after each of them, the capacitor is discharged through one of the resistors R_{c1}, R_{c2} or R while the pins connected to the two other resistors are in high impedance state, HZ. The discharges end when the Pp pin (configured in these discharges as input) detects a logic 0 when the threshold voltage V_{Th} has been reached. Finally, the PDD measures and stores, in number of clock cycles, the discharge time through the resistors. This time for R is given by

$$T_R = (R + R_o) C \ln\left(\frac{V_{DD}}{V_{Th}}\right) \quad (1)$$

where R_o is the output resistance of each pin configured as logic 0 output. Using (1) and the analogous equations for the discharges through R_{c1} and R_{c2} (T_{Rc1} and T_{Rc2}), we can find R [29],

$$R = \frac{T_R - T_{Rc1}}{T_{Rc2} - T_{Rc1}}(R_{c2} - R_{c1}) + R_{c1} \quad (2)$$

Using (2), the influence of C, V_{DD} and V_{Th} in calculating R is eliminated, and its value only depends on known resistances and on measuring three discharge times.

The second type of DIC is the Three Signals Method (TSM) shown in Fig. 1 (b). Its operation is very similar to the TPCM, but in this case by configuring the pins so the discharges occur through R_{c1}, $R_{c1} + R_{c2}$ and $R + R_{c1}$. Estimation of R is obtained through [29],

$$R = \frac{T_{R+Rc1} - T_{Rc1}}{T_{Rc1+Rc2} - T_{Rc1}} R_{c2} \quad (3)$$

where $T_{Rc1+Rc2}$ is the discharge time through $R_{c1} + R_{c2}$.

From a computational point of view, the TSM requires fewer arithmetic operations and stores the value of a single resistor instead of two, unlike the TPCM. However, the $T_E(R)$ for the TPCM and the TSM ($T_{E,TPCM}(R)$ and $T_{E,TSM}(R)$, respectively) are related by [14],

$$T_{E,TSM}(R) \approx T_{E,TPCM}(R) + T_{Rc1} \quad (4)$$

and the uncertainties in estimating R in both methods, $u_{TPCM}(R)$ and $u_{TSM}(R)$ by

$$u_{TPCM}(R) < u_{TSM}(R) \tag{5}$$

Considering that the difference in the computational cost of (2) and (3) is minimal, the benefits of the TPCM therefore outperform those of the TSM.

As indicated above, $T_E(R)$ increases linearly with R in both the TPCM and in the TSM, which can be a problem if the resistances to be measured are high. To mitigate this problem, a new calibration method [14] has recently been introduced, namely the Fast Calibration Method (FCM), which also uses the circuit of Fig. 1 (a), just like the TPCM. However, this method, under certain circumstances, divides the discharge process into two parts to find T_R: the first part through the R sensor itself, and the second part through R_{c1}. This is called the *modified discharge procedure*, in order to distinguish it from the *normal discharge procedure* through a single resistor. In the modified discharge procedure, the first part of the discharge is made through R and has a duration set by the designer, T_x, which is a number of PDD clock cycles. Discharge continues through R_{c1} if T_x is reached during discharge through R without reaching a logic 0 on the Pp pin. In this case, if $R > R_{c1}$, discharge through R_{c1} will be faster than if it continued through R, thus reducing the time needed to find T_R.

If we call $T'_{Rc1}(R)$ the time that the discharge lasts through R_{c1} in the modified procedure of discharging R, then the time that would have been employed in carrying out discharge completely through R only can be found according to the following expression [14]:

$$T_R = \frac{T_{Rc1}}{T_{Rc1} - T'_{Rc1}(R)} T_x \tag{6}$$

In the FCM, the lower the value of T_x and the higher the value of R, the reduction in time needed to find T_R increases. However, this process is associated with a small increase in the uncertainty of T_R, and therefore also brings increased errors in estimating R. Fortunately, there are combinations of T_x values with ranges of R values that show a very small increase in errors, or even ensure they are not increased. Considering (2) and (6), the simplest version of the FCM uses the following equation to calculate R:

$$R = \begin{cases} \dfrac{T_R - T_{Rc1}}{T_{Rc2} - T_{Rc1}}\left(R_{c2} - R_{c1}\right) + R_{c1}, & T_R < T_x \\ \dfrac{T_{Rc1}}{T_{Rc1} - T'_{Rc1}(R)} T_x - T_{Rc1} \\ \dfrac{}{T_{Rc2} - T_{Rc1}}\left(R_{c2} - R_{c1}\right) + R_{c1}, & T_R \geq T_x, \end{cases} \tag{7}$$

However, for low resistances, one of the main causes of error in estimating R, for any of the methods presented, is uncertainty due to quantization. Indeed, since they are low resistances, an important drop in capacitor voltage can occur during discharge in a clock cycle of the PDD. Therefore, it may be that uncertainty in measuring T_R can be 0 and, in contrast, there is a significant error in measuring R. This situation occurs if the voltage drop in a cycle is greater than any variations due to the circuit's electrical noise. It is obvious that, by increasing C, noise reduction can be achieved due to reducing quantization error. However, this solution, besides having practically no effect on the middle and high part of the resistance range, increases $T_E(R)$ by increasing T_R, T_{Rc1} and T_{Rc2}. Naturally, the operating frequency of the PDD can also be increased, but this may be limited by the PDD itself, and also implies an increase in power consumption and electrical noise, causing errors in the measurements.

Designing a DIC that manages to reduce measurement error due to quantification in low resistance values therefore becomes an interesting technological challenge. In the next section, we will present a DIC that achieves this reduction.

III. Calibration Method for Error Reduction in the Readout of Low Resistances

This section presents a new DIC based on the modified discharge procedure characterized by (6), with the aim of reducing errors in estimating lower resistances. We call this new method *Quantization Error Reduction Method* (QERM).

QERM uses the DIC shown in Fig. 2. The circuit topology, the way in which the discharges are produced and controlled, and the use to be given to the Pc1 pin are the main differences between the QERM and the TPCM, the TSM or the FCM. The process of estimating R involves three charging and discharging processes, just like the other methods. The order is indifferent, but there is one discharge for resistor R_{c1}, labelled as discharge (A) in Fig. 2, and another for $R_{c1} + R_{c2}$ indicated as (B) in Fig. 2 (as in the TSM, the sum $R_{c1} + R_{c2}$ plays the role of second calibration resistor). The remaining discharge is initiated simultaneously through R and $R_{c1} + R_{c2}$, indicated as C_R and C_C in Fig. 2, and, in an instant of this discharge, it continues only through R (discharge C_R) or through $R_{c1} + R_{c2}$ (discharge C_C). For its part, resistor R_p performs the same function as in the previous methods. If a PDD pin does not participate in a discharge process, it will be configured as input (equivalent to a *HZ* state).

During the simultaneous discharge process through Ps and Pc2 (from now on simultaneous discharge), the Pc1 pin, configured as input, is used to find the instant at which V_A in Fig. 2 reaches V_{Th}. Notation T_A is used to represent the time from the start of the simultaneous discharge to the time when $V_A = V_{Th}$. T_S is defined as the measured time of a simultaneous discharge, if it is completed until the voltage in the capacitor reaches V_{Th} (although this discharge is not really performed in the QERM). Likewise, T_L is a time selected by the designer that is used to determine if simultaneous discharge ends only through R or $R_{c1} + R_{c2}$. During simultaneous discharge, if $T_A < T_L$, from T_A capacitor discharge continues only through $R_{c1} + R_{c2}$. However, if during simultaneous discharge, V_A has not dropped to V_{Th} after a time interval T_L (which implies that $T_A \geq T_L$), from T_L capacitor discharge continues only through R. Table I summarizes the state of pins during the discharge stage. In the charging process all pins are logic 1 outputs.

If discharge ends through R, T'_R is the time interval during which discharge is performed through R. If discharge is terminated by $R_{c1} + R_{c2}$, T'_C is the discharge time only through $R_{c1} + R_{c2}$. Fig. 3 illustrates these two types of discharge and

the associated temporal parameters. This figure also shows that T_L must verify that $T_L < T_{Rc1+Rc2}$.

TABLE I
PINS CONFIGURATION FOR EACH OF THE MEASUREMENTS CARRIED OUT BY THE CIRCUIT IN FIG. 2

Measurement	Ps	Pc1	Pc2	Pp
R_{c1}	*Hz*	*"0"*	*Hz*	*Hz*
$R_{c1}+R_{c2}$	*Hz*	*Hz*	*"0"*	*Hz*
R when Pc1 input = "1"	*"0"*	*Hz*	*"0"*	*Hz*
R when Pc1 input = "0" and $T_A < T_L$	*Hz*	*Hz*	*"0"*	*Hz*
R when Pc1 input = "0" and $T_A \geq T_L$	*"0"*	*Hz*	*Hz*	*Hz*

The T_L parameter is chosen to distinguish between low resistances and the others. If R is low, simultaneous discharging is faster, meaning $T_A < T_L$ for an appropriate T_L selection. In this situation, the trigger instant in Ps for the proposed DIC occurs when discharge takes place through $R_{c1} + R_{c2}$, meaning quantization error is small, since the sum of these two resistors is large. A good practice is to use values of R_{c1} close to $0.15 \cdot R_{max}$ and $R_{c1} + R_{c2}$ close to $0.85 \cdot R_{max}$ (R_{max} is the maximum resistance in the range) [8], [30]. On the other hand, if $T_A \geq T_L$, discharge can finish through R as it is not a low resistance, so quantization error is small.

The value of R through the circuit of Fig. 2 can be found with the following equation, obtained using (1) for R, R_{c1} and $R_{c1} + R_{c2}$

$$\frac{T_R - T_{Rc1}}{T_{Rc1+Rc2} - T_{Rc1}} = \frac{R - R_{c1}}{R_{c2}} \tag{8}$$

after solving for R

$$R = \frac{T_R - T_{Rc1}}{T_{Rc1+Rc2} - T_{Rc1}} R_{c2} + R_{c1} \tag{9}$$

The only problem when using (9) is that T_R is not directly available, since discharge only through R is not carried out in the QERM. However, we can use the measurements of the simultaneous discharge times to find this unknown quantity. Firstly, if a discharge were made only through R (although this is not the case in this method), T_R would be related to T_S according to the following expression:

$$\frac{1}{T_S} = \frac{1}{T_R} + \frac{1}{T_{Rc1+Rc2}} \tag{10}$$

where the different times have been obtained from equations equivalent to (1). Although T_S is not measured in the QERM, it is possible to find its value using the equation of the modified discharge procedure (6) adapted to the two situations which determine the values of T_A and T_L. Thus, if $T_A < T_L$, we can find T_S by the following adaptation of (6):

$$T_S = \frac{T_{Rc1+Rc2} \cdot T_A}{T_{Rc1+Rc2} - T_C'} \tag{11}$$

Using this value of T_S in (10) and defining $T_{S-C} = T_A + T_C'$, obtains the value of T_R

$$T_R = \frac{T_{Rc1+Rc2} \cdot T_A}{T_{Rc1+Rc2} - T_{S-C}} \tag{12}$$

All parameters on the right side of this equation are known in the QERM. If $T_A \geq T_L$, a new adaptation of (6) provides a second relationship between T_R and T_S,

$$T_S = \frac{T_R \cdot T_L}{T_R - T_R'} \tag{13}$$

Replacing this value of T_S in (10) and defining $T_{S-R} = T_L + T_R'$, will obtain the expression of T_R in this situation,

$$T_R = \frac{T_{Rc1+Rc2} \cdot T_{S-R}}{T_{Rc1+Rc2} - T_L} \tag{14}$$

where again, the parameters on the right side in (14) are known in the QERM.

Finally, using (9), (12) and (14) we can establish the equation that gives us the estimation of R in the QERM

$$R = \begin{cases} \dfrac{\dfrac{T_{Rc1+Rc2} \cdot T_A}{T_{Rc1+Rc2} - T_{S-C}} - T_{Rc1}}{T_{Rc1+Rc2} - T_{Rc1}} R_{c2} + R_{c1}, & T_A < T_L \\ \dfrac{\dfrac{T_{Rc1+Rc2} \cdot T_{S-R}}{T_{Rc1+Rc2} - T_L} - T_{Rc1}}{T_{Rc1+Rc2} - T_{Rc1}} R_{c2} + R_{c1}, & T_A \geq T_L \end{cases} \tag{15}$$

As we have seen, the QERM does not require any additional hardware compared to traditional calibration methods or the FCM. However, programming of the PDD should be different for this method, since one comparison and one multiplication and division are needed in addition to, for example, what the TPCM requires (it should be noted that T_{S-C} and T_{S-R} can be obtained directly from a counter).

From the point of view of $T_{E(R)}$, if $T_A < T_L$, according to the upper term of (15), T_{S-C} needs to be measured in order to estimate T_R. This situation occurs for small values of R and, in this case, T_A is very similar to the time that would be measured by discharging only through R, for V_A reaching V_{Th}. However, discharge through $R_{c1} + R_{c2}$ from this moment is always slower than through R. Therefore, in general more time is needed for estimating low R values in the QERM than using the other methods. However, for high resistances with values above $R_{c1} + R_{c2}$, $T_{E(R)}$, using the QERM, $T_{E,QERM(R)}$, is always shorter than $T_{E,TPCM(R)}$. In particular, maximum estimation

time using the QERM, $T_{E,QERM}(R_{max})$, is shorter than for the TPCM, and this is usually the main time parameter in most applications.

As indicated in [7], power consumption in a DIC depends basically on the number of discharges of the capacitor for the estimation R and of the product $f_{CK} \cdot C$, where f_{CK} is the clock frequency of the PDD. Since the QERM needs the same number of discharges as the other methods, its power consumption should be equal. However, reducing quantization error minimizes either the operating frequency or C in order to obtain the same uncertainty as in the other methods, making it a more efficient calibration method for an uncertainty-power consumption relationship.

IV. Materials and Methods

The proposed method was tested with a circuit based on a Xilinx Spartan 6 FPGA (XC6SLX25-3FTG256) [35] which works with independent supply voltages for the input/output blocks and the digital processing core, which is why two regulators (TPS79912 and TPS79633, Texas Instruments, Dallas, TX, USA) are used to power the core of the device at 1.2 V and the I/O buffers at 3.3 V. This limits the noise that digital activity can generate on the device's input and output pins. The maximum current an output buffer of the FPGA can sink to maintain the digital signal integrity of the outputs is 24 mA. The PCB the circuit is mounted on has been manufactured with an FR-4 fiberglass substrate and four layers, leaving internal layers for supply planes and external layers for the remaining signals.

Experimental tests were performed for 24 resistors with resistance values within the range 33 Ω to 8169 Ω, while a capacitor with a 47 nF nominal value was selected. This value of C has been chosen so the discharge times are not excessively long and can be determined with a 14-bit counter, while providing sufficient measurement accuracy [6] (the maximum discharge time for the capacitor with these choices is 327.28 µs). In addition to the resistor to be measured, there were two additional calibration resistors: R_{c1} = 1099.2 Ω and R_{c2} = 5073.7 Ω. Note that equivalent R_{c2} for the TPCM is the sum of R_{c1}+ R_{c2}: 6172.9 Ω. Given the careful design aimed at minimizing electrical noise, and also in order to use the shortest possible time in the charge cycles, R_p = 0 Ω has been selected. All the resistors were measured using an Agilent 34401A digital multimeter. A total of 500 measurement cycles were performed for each of the 24 resistors used in order to measure the maximum errors and uncertainties. These 500 cycles were repeated each time the resistors are estimated using the two different calibration methods. In each cycle, the discharges were also carried out through the calibration resistors.

V. Experimental Results and Discussion

In order to evaluate the performance of the QERM, the measurements obtained by the circuit shown in Fig. 2 have been compared with those obtained by the TPCM. The TPCM is used for comparison rather than the FCM or the TSM since, for low resistances, the TPCM is identical to the FCM, and, as commented, $T_{E,TPCM}(R) < T_{E,TSM}(R)$ and $u_{TPCM}(R) < u_{TSM}(R)$, making the TPCM more interesting, in practice, than the TSM. Comparisons have been made at different system clock frequencies in order to clarify the effects of quantization. Fig. 4 and Fig. 5 show the results obtained by comparing Maximum Absolute Error (in ohms), *MAE(R)*, and Maximum Relative Error (in percentage), *MRE(R)*, defined as:

$$MAE(R) = \left| Inferred\ Value(R) - Actual\ Value(R) \right|$$
$$MRE(R) = 100 \cdot \frac{MAE(R)}{Actual\ Value(R)} \quad (16)$$

It is important to note that, in both figures, the maximum resistance measured by the QERM and the TPCM differ. This is due to the fact that, when measuring a resistance value of the high part of the range ($T_A \geq T_L$) using the QERM, part of the discharge is carried out in parallel through R and R_{c1} + R_{c2}. Total time until the logic 0 is detected in Ps is therefore less than if the discharge were made only through R, as in the TPCM. Since the counter used to measure this time is identical for both methods (a 14-bit counter), the maximum resistance that can be measured for a frequency of 50 MHz is 7464 Ω for the TPCM and 8169 Ω for the QERM. It should also be noted that Fig. 4 and Fig. 5 show results for the QERM for both T_L = 10 µs and for T_L = 20 µs at several frequencies.

The first thing to consider in Fig. 4 is that, although the QERM has been designed to improve errors in the low resistances measurement, there is also a better result in high resistances. The explanation of this phenomenon must be related to the different leakage capacitances that appear in the circuits of Fig. 1 (a) and Fig. 2. In any case, the difference between the methods becomes smaller as the resistance decreases to medium values, and the differences between both methods are very small in the central resistances zone for all f_{CK} of Fig. 4. The differences that appear for low resistances are therefore caused by the reduction in quantization noise in the QERM. In Fig. 4 (a), for f_{CK} = 12.5 MHz the greatest difference between both methods is observed for low resistances. This is logical since quantization noise is higher at lower clock frequency, and the level of noise floor introduced by the clock is lower. Moreover, this figure shows that errors in the TPCM are very different, since the quantization error of a given resistance depends on when the trigger occurs within the clock cycle. Thus, there are resistance values that are always measured with error greater than others. As expected, in Fig. 4 (b) and Fig. 4 (c) the difference in the errors decreases due to the higher frequencies used. Moreover, in Fig. 4, the QERM shows a practically constant error for all the resistances of the lower part of the range, since, with this method, quantization error is clearly below the other circuit noises.

However, the difference between QERM and TPCM errors decreases as clock frequency increases because quantization error also does so. Nevertheless, the decrease in quantization error does not reduce the total noise level due to the increase of the noise floor caused by a higher frequency clock. The QERM therefore has optimal measurement frequencies for low resistances. In other words, since power consumption is related to the product $f_{CK} \cdot C$, it will also have an optimal value for estimating low resistances.

On the other hand, in the QERM the curves with T_L = 10 µs and T_L = 20 µs coincide for resistance values below 468 Ω, since for this resistance $T_A \approx 10$ µs (with any of the clock frequencies). However, both values of T_L provide different estimations for higher resistances. Nevertheless, we see how this only slightly changes the estimations in the central part of the resistance range.

Fig. 5 shows the same information as in Fig. 4 (a) but using Maximum Relative Error, *MRE(R)*. This figure illustrates more clearly the performance of the QERM when compared to the TPCM. In the high resistance values zone, the relative errors of both methods are very small and similar to each other. However, the relative error in both methods increases as the resistance to be measured decreases. This increase is mainly related to variations in R_o when discharging through low resistances [36]. Nevertheless, in the QERM the error increases smoothly, meaning the relative error of the QERM is 1.56% for the lower resistance of the range, while for the TPCM it is 3.77%.

The systematic error of both methods for f_{CK} = 12.5 MHz, calculated as the difference between the average value of the 500 measurements and the actual value, is shown in Fig. 6. The behavior of these systematic errors for both methods is identical to that shown by the maximum errors of Fig. 4 (a). However, in Fig. 6, for the resistances range between 33 Ω and 747 Ω, the maximum systematic error for the QERM is 0.33 Ω for both T_L = 10 µs and T_L = 20 µs, while the TPCM has a maximum systematic error in this resistances range of 1.44 Ω. Fig. 7 shows the uncertainties (in ohms) in the estimation of the resistance. In this case, there are no significant differences between the methods. These uncertainties have the typical behavior that appears in a resistive DIC, increasing with the resistance value to be estimated.

VI. Conclusion

Direct Interface Circuits are a simple and efficient alternative to perform the reading of resistive sensors and provide it in digital format. This task is done through a resistance-to-time-to-digital conversion. Conversion can be carried out by different methods. These methods differ in the accuracy of the measurements, the complexity of the arithmetical calculations, and the time needed to perform the conversion. Although all methods use reduced hardware and accuracy for high and medium resistances is quite good, they also share the fact that relative error of the estimation is notably increased for low resistances, mainly due to quantization error.

In order to improve this kind of error, this article presents a new DIC architecture (which does not require additional elements) and a new measurement method that we call Quantization Error Reduction Method, QERM. Together, they provide a reduction in quantization error, and therefore obtain better estimations for low resistances while maintaining performance for the rest of the resistance range. The basic idea of the QERM is to divide the capacitor discharge that is used to estimate the resistance into two parts. In the first part, the discharge is carried out simultaneously through the resistor to be measured and the calibration resistors, while in the second part it is discharged only through these calibration resistors if R is low. Otherwise, it is discharged only through R. Discharge therefore always occurs through a high resistance at the right time. The circuit has been implemented using an FPGA operating at different clock frequencies. The errors obtained are, at most, 0.33 Ω in the range between 33 Ω and 747 Ω. The maximum relative error for this same range is 1.56%, which is less than half that obtained by using the traditional two-point calibration method, for an operating frequency of 12.5 MHz.

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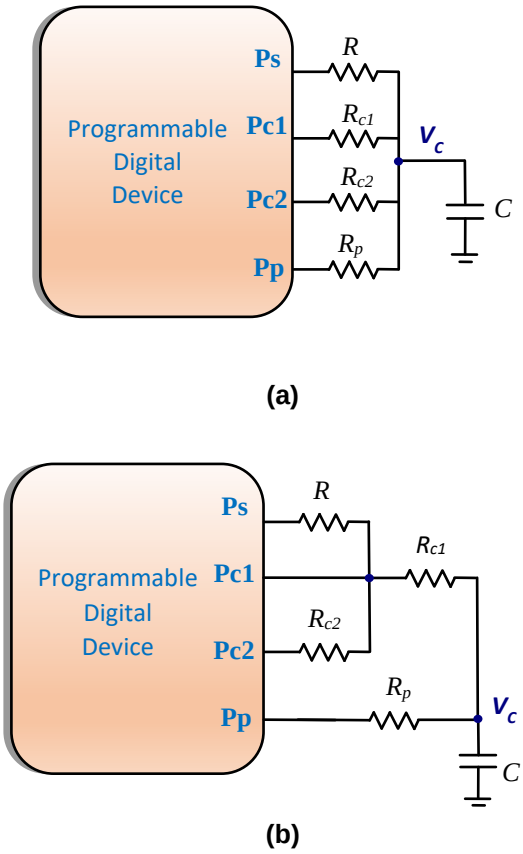


Fig. 1. **(a)** Circuit used in the *Two Point Calibration Method (TPCM)* and *Fast Calibration Method (*FCM*)*. **(b)** Circuit used in the *Three Signal Method (TSM).*

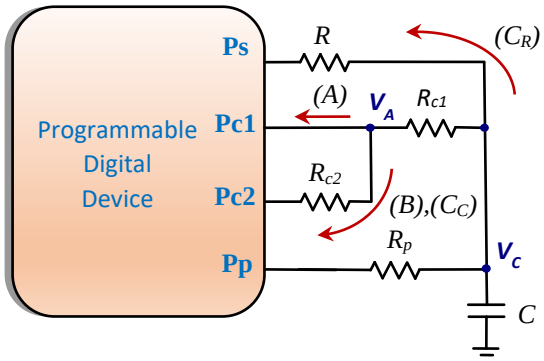


Fig. 2. Proposed Direct Interface Circuit to reduce quantization error effects for low value resistors. The arrows show the paths for the three different discharge cycles. Discharges through C_R and C_C begin simultaneously but end with only one of them.

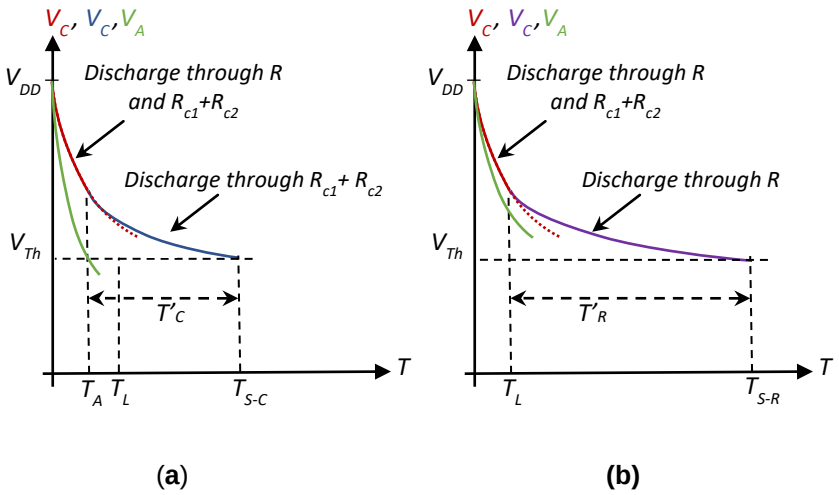
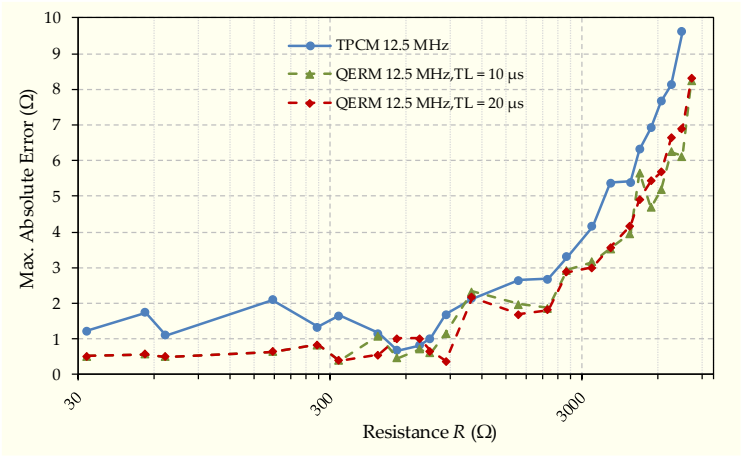
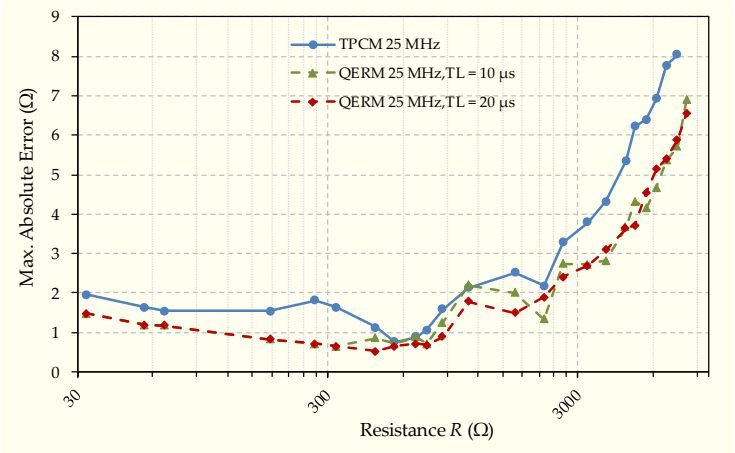


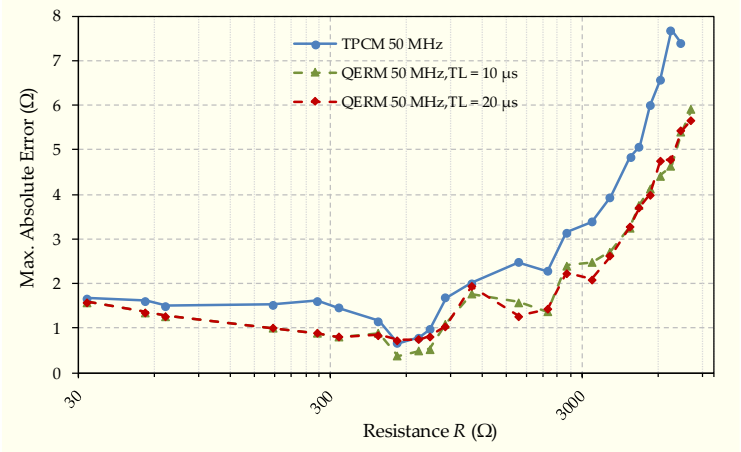
Fig. 3. Evolution of capacitor voltage, V_C, in final discharges through R_{c1} + R_{c2} (blue) or R (purple). Evolution of V_A voltage of Fig. 2 is also shown. **(a)** If $T_A < T_L$, the simultaneous discharge process ends when $V_A = V_{Th}$, then discharge continues through R_{c1} + R_{c2}. **(b)** If $T_A \geq T_L$, the simultaneous discharge process ends at T_L, then discharge continues through R.



(a)



(b)



(c)

Fig. 4. Maximum Absolute Error (in Ω) for the TPCM (blue continuous line) and for the QERM with T_L = 10 µs (green dashed line) and T_L = 20 µs (red dotted line). X-Axis, in all figures, is in log10 scale. **(a)** The clock frequency, f_{CK}, used in the circuit is 12.5 MHz, **(b)** f_{CK} = 25 MHz and **(c)** f_{CK} = 50 MHz.

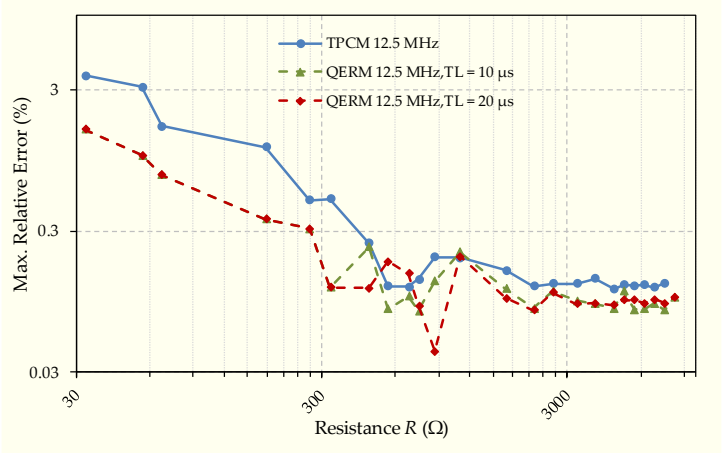


Fig. 5. Maximum Relative Error (in % and logarithmic scale) for the TPCM (blue continuous line) and for the QERM with T_L = 10 µs (green dashed line) and T_L = 20 µs (red dotted line). X-Axis is in log10 scale. The clock frequency, f_{CK}, used in the circuit is 12.5 MHz.

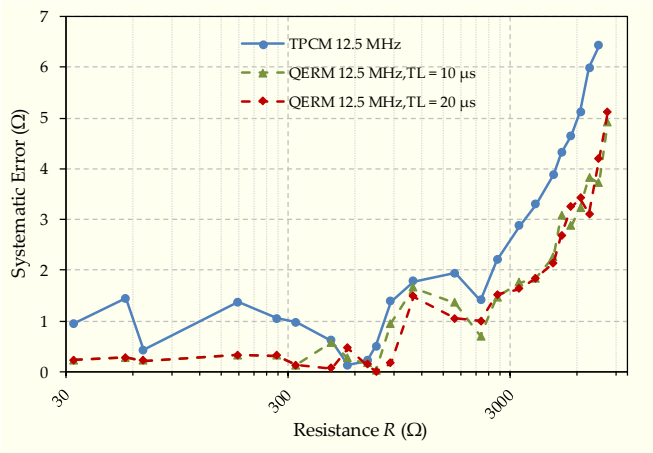


Fig. 6. Systematic Error (in Ω) for the TPCM (blue continuous line) and for the QERM with T_L = 10 µs (green dashed line) and T_L = 20 µs (red dotted line). X-Axis is in log10 scale. The clock frequency, f_{CK}, used in the circuit is 12.5 MHz.

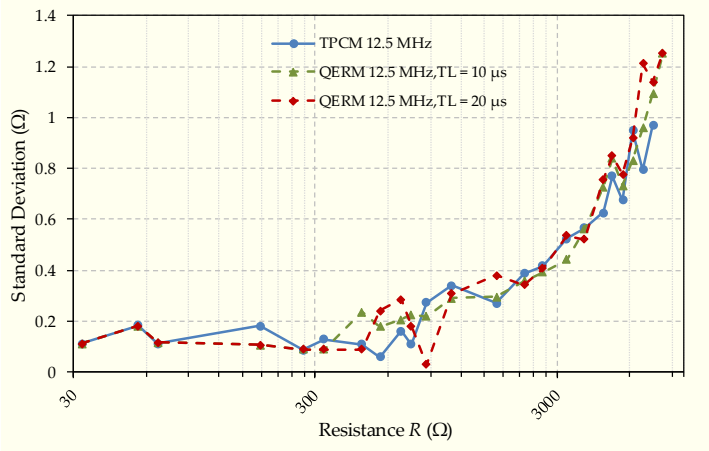


Fig. 7. Standard Deviation (in Ω) for the TPCM (blue continuous line) and for the QERM with T_L = 10 µs (green dashed line) and T_L = 20 µs (red dotted line). X-Axis is in log10 scale. The clock frequency, f_{CK}, used in the circuit is 12.5 MHz.