Broadband 1-bit Reconfigurable Intelligent Surface at Millimeter Waves: Overcoming PIN-Diode Degradation with Slotline Ring Topology

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***Abstract*—This paper explains the non-idealities that arise when using PIN diodes at millimeter-wave frequencies and the important limitations that they bring in classical configurations of 1-bit slotline reconfigurable unit cells. A robust solution is proposed where a single PIN diode is inserted inside a ring topology. The slotline unit cell is analyzed through a circuit-model approach. Its performance is compared with a unit cell based on a single slotline, which also includes a PIN diode, referred to as classical configuration. For experimental assessment, a circuit prototype is fabricated to verify the phase difference of both PIN diode states in each unit cell configuration. The measured results reveal that the slotline unit cell with ring configuration provides a $180^\circ \pm 20^\circ$ reflection phase difference from 36.3 GHz to 45 GHz (21.4% relative bandwidth). Finally, the proposed slotline unit cell with ring topology is measured in a complete array to assess its performance in periodic and quasi-periodic environments. The measurements confirm the 1-bit behavior for both normal and oblique incidence with losses less than 2 dB. Therefore, this enables the design of wideband 1-bit reconfigurable reflectarrays and RIS in this frequency range.**

***Index Terms*—1-bit reconfiguration, broadband, millimeter waves, PIN diode, reconfigurable intelligent surface (RIS), slotline technology, unit cell.**

I. Introduction

With the increasing demand for wireless communications in 5G and the emergence of 6G, millimeter-wave frequencies have become essential due to the congestion of the sub-6 GHz spectrum [1]. To support this shift, new radio-frequency (RF) components operating in the millimeter-wave range must be developed. Currently, specific frequency bands between 24.75 GHz and 43.5 GHz (corresponding to 5G bands n257 to n261) have been allocated. In these bands, key RF components such as antennas [2]–[4], phase shifters [5], [6], and amplifiers [7], [8] are being actively proposed.

Reconfigurable intelligent surfaces (RIS) have recently garnered significant attention as a promising technology for the future of wireless communications [9], [10]. These devices enable smart control of electromagnetic (EM) wave reflections in the wireless environment, enhancing communication links by mitigating challenges such as severe path loss and blockages—issues that are particularly critical at millimeter-wave frequencies. RIS reconfigurability can be achieved using various elements, including varactors [11], [12], reconfigurable materials [13], [14], and PIN diodes [15]–[19]. Among these, PIN diodes are the most widely used due to their low complexity and power consumption [20]. However, implementing RIS with PIN diodes at millimeter-wave frequencies presents challenges, as the switch behavior of PIN diodes deteriorates at higher frequencies.

To date, only a few works have successfully developed PIN diode-based RIS operating near 30 GHz. For example, in [21], a RIS unit cell for a frequency band around 28.5 GHz was designed using a patch coupled to a parasitic resonator controlled by a PIN diode, achieving 1-bit reconfiguration (180° reflection phase shift) over a 2 GHz bandwidth. Similarly, the RIS element proposed in [22] demonstrated 1-bit behavior across the 22.7 GHz to 30.5 GHz frequency range. Furthermore, [23] introduced the design and fabrication of a RIS element capable of 2-bit reconfiguration (90° phase shift) at around 29 GHz.

Reconfigurable reflectarrays, which share many similarities with RIS, have also employed PIN diode-based unit cells for operation in the V-band. For example, the unit cell presented in [24] utilizes a patch antenna and a stub controlled by a PIN diode to achieve 1-bit reconfiguration at 60.25 GHz. Nevertheless the 1-bit reconfiguration bandwidth is only 450 MHz. More recently, [25] demonstrated a unit cell capable of 1-bit reconfiguration over a 5 GHz bandwidth at approximately 72.8 GHz, corresponding to a 6.8% relative bandwidth, while maintaining acceptable reflection losses. This design relies on polarization conversion for the 180º phase shift and thus, it requires two PIN diodes per unit cell. Despite these advancements, there remains a gap in the literature regarding the design of reflective unit cells capable of broadband recon-

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figurable phase shift in millimeter-wave bands using a single PIN diode.

The slotline ring has been used for decades in many antenna designs [26]. Primarily, the slotline ring has been used as an individual antenna fed by a conventional feeding line and port where its radiation characteristics could be controlled by diodes [27]. However, so far, its potential has been scarcely explored in unit cells for spatially-fed antennas where the slotline ring structure is not used as a radiating element. In this paper, we propose a new kind of reconfigurable unit cell that provides 1-bit reconfiguration with broadband performance for frequencies around 40 GHz. The 40 GHz frequency band has been chosen because it is around n259 (39.5 GHz - 43.5 GHz) and n260 (37 GHz - 40 GHz) bands which are proposed by 3GPP for 5G FR2 [28]. The used reconfigurable element is a single PIN diode, so it is necessary to employ a technology that contains substrate and metal. Slotline is chosen because it facilitates the soldering of the PIN diode between the metals and also presents an interesting potential for producing reflective unit cells [29]. Unlike other 1-bit unit cells for reconfigurable reflectarrays or RIS at millimeter-wave frequencies, the presented unit cell relies on an original implementation where a slotline ring is asymmetrically loaded by a single PIN diode. This particular configuration enables overcoming PIN diode limitations at higher frequencies thus, leading to a 1-bit phase-shifter with improved performance. The main challenge addressed by the proposed slotline unit cell is the bandwidth degradation for the 1-bit reconfiguration when operating frequency reaches the millimeter-wave frequencies. It achieves a relative bandwidth of 21.4% with reflection losses similar to what is found in the state of the art. The remainder of this paper is organized as follows. Section II presents the two designs of slotline unit cells with phase reconfiguration in reflection at millimeter waves. A comprehensive analysis of their EM performances from 35 GHz to 45 GHz is carried out. In Section III, the experimental verification of both reconfigurable slotline unit cells is performed along with their comparison and the discussion of obtained results. This section also provides the experimental demonstration of the 1-bit performance of the proposed slotline unit cell in an array environment. Finally, conclusions are drawn in Section IV.

II. Switching capability in slotline unit cells

A. PIN diode degradation at millimeter waves

At high frequencies, the states of a PIN diode can be modeled by equivalent circuits [30]. In the ON state, the PIN diode can be modeled as an inductor (with value L_d) in series with a resistor (with value $R_{d,ON}$). While in the OFF state, the PIN diode is modeled with the inductor L_d in series with a parallel of a resistor and capacitor whose values are $R_{d,OFF}$ and $C_{d,OFF}$, respectively. In the latter parallel circuit, mainly the effect of $C_{d,OFF}$ dominates because $R_{d,OFF}$ is of the order of hundreds of kΩ. Table I lists the most used commercial PIN diode models for RIS and reconfigurable reflectarray designs at microwave and millimeter-wave frequencies. Table I also includes the main values of the equivalent circuit for the PIN diode states. Reconfigurable designs at frequencies near 30 GHz use the PIN diode models with the lowest values for L_d and $C_{d,OFF}$. In fact, for $C_{d,OFF}$, the lowest values that commercial PIN diodes can provide are around 40 fF. It is important to note that although in the datasheet of the MADP-000907, MA4AGBLP912, MA4AGFCP910, and MA4AGP907 models the $C_{d,OFF}$ is between 20 fF and 30 fF, due to the packaging, this value increases up to 40 fF [31]. To quantify the impedance change provided by a commercial PIN diode over frequency, Table II presents the resulting impedances of both states for the MA4AGP907 PIN diode [32]. The ON and OFF states of the PIN diode are different in terms of impedance since they are intended to be similar to a short circuit and an open circuit, respectively. Table II shows the evolution of these impedances at several frequencies. It can be observed how both states change as the frequency increases. In particular, the OFF state changes drastically, since the PIN diode does not behave any more as an open circuit at 40 GHz. This implies an important degradation of the desired switching behavior of the PIN diode, and this justifies why it is hardly employed at millimeter waves.

TABLE I: List of commercial PIN diodes for microwave and millimeter-waves applications and reported equivalent circuits

Ref.	Frequency (GHz)	PIN Model	L_d (pH)	$R_{d,ON}$ (Ω)	$C_{d,OFF}$ (fF)
[15]	3.75	SMP1321-040LF	450	3	180
[16]	5	SMP1345-079LF	700	3	120
[18], [21], [22], [23]	28	MADP-000907	30	7.8	35
[19]	28	MA4AGP907	50	4.2	42
[24]	60.25	MA4AGBLP912	30	8	27*
[25]	72.8	MA4AGFCP910	10	4	45

* Does not take into account the effect of packaging.

TABLE II: Impedance of MA4AGP907 PIN diode at different frequencies

State	At 3.5 GHz	At 10 GHz	At 40 GHz
ON	$5.12e^{j12.4^o}$ (Ω)	$5.9e^{j32.1^o}$ (Ω)	$13.52e^{j68.3^o}$ (Ω)
OFF	$1.14e^{-j89.7^o}$ (kΩ)	$396.8e^{-j89.9^o}$ (Ω)	$98.37e^{-j90^o}$ (Ω)

B. Limitations of classical configuration

The most intuitive configuration to conceive a reconfigurable PIN diode-based 1-bit unit cell is analyzed in Fig. 1. Such a proposal is based on the static reflected phased behavior proposed in [29], which depends on the effective electric length of a short-circuited slotline. For a concise and efficient analysis of this unit cell, the excitation from free space has been replaced by an equivalent excitation through a port placed at the beginning of the slotline. In this way, the fundamental quasi-TEM mode is successfully generated, avoiding any reflection between free space and the unit cell. To compatibilize the excitation through a port with periodic conditions along the $x-$ and $z-$directions, PEC-PMC conditions have been applied, as illustrated in Fig. 1(a). The substrate considered is RO4003C ($\varepsilon_r = 3.55$ and thickness

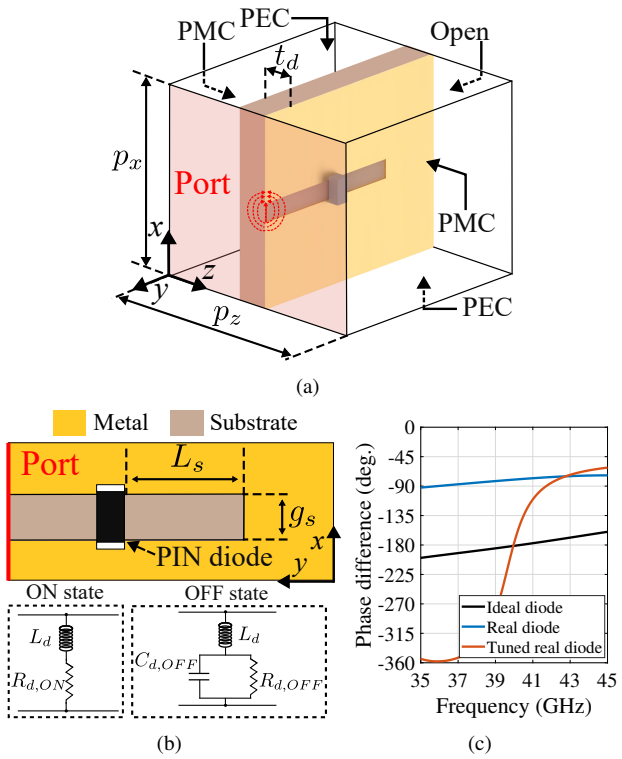

Fig. 1: Classical configuration of the 1-bit slotline unit cell: (a) 3D view, (b) Planar view with the equivalent circuits for the PIN diode and, (c) Phase difference versus frequency. The dimensions (in mm) are: $p_x = p_z = 3$, $g_s = 0.3$, $L_s = 1.5$ (for ideal/real case) and 2.9 (for tuned real case). Values for the real PIN diode [32]: $L_d = 50$ pH, $R_{d,ON} = 5\ \Omega$, $R_{d,OFF} = 200\ k\Omega$, and $C_{d,OFF} = 40$ fF.

t_d is 0.508 mm) and the EM software used to compute the simulated results is CST Studio Suite 2024.

Fig. 1(b) shows the planar view of the unit cell of Fig. 1(a). To achieve a 1-bit reconfiguration between PIN diode states, a 180º phase difference in the reflected wave at the port must be obtained. In this configuration, the position of the PIN diode (marked by L_s in Fig. 1(b)) is critical. From a circuit point of view, this unit cell can be modeled as two transmission lines in series, where the second line has length L_s and ends in short circuit. Between these two lines is the admittance of the PIN diode. If the PIN diode was ideal, i.e., providing perfect short-circuit and open-circuit states, the value of L_s would be $\lambda_s/4$, with λ_s being the wavelength in the slotline at the center frequency. Fig. 1(c) shows the simulated phase difference results versus frequency. In the case of an ideal PIN diode, this $\lambda_s/4$ segment actually provides a phase difference of 180º with a variation of ±20º from 35 GHz to 45 GHz. However, when considering the values found in a real PIN diode, this phase difference is far from the desired [see blue curve in Fig. 1(c)]. Albeit, by assuming real diode values and adjusting the value of L_s, this 1-bit performance between PIN diode states can be achieved. This can be seen in the orange curve in Fig. 1(c), where the 180º phase difference is reached at 40 GHz. Unfortunately, the phase difference behavior is narrowband (around 400 MHz bandwidth). Moreover, this unit cell configuration has other disadvantages such as: (i) any tolerance in L_s has a large impact on the frequency where the 1-bit reconfiguration occurs and, (ii) the need for a decoupling structure on the slotline metal in order not to short circuit the PIN diode terminals when applying the DC bias.

C. Efficient switching with ring configuration

Fig. 2(a) shows the slotline unit cell design proposed in this work to overcome all the shortcomings mentioned for the classical configuration. A planar view of the proposed unit cell is illustrated in Fig. 2(b). Now, the design consists of a slotline terminated in a slotline ring where the PIN diode is placed, connecting the metals which form the ring as seen in Fig. 2(b). The area where the input slotline, which is connected to the port, meets the ring is a slotline junction illustrated in Fig. 2(c). For the sake of understanding, we are going to carry out a circuit analysis of this unit cell configuration. In this way, an equivalent circuit that can efficiently predict the EM behavior of the proposed unit cell will also be derived. The equivalent circuit for the ring configuration is shown in Fig. 3(a). It consists of a transmission line with characteristic impedance Z_s (it models the input slotline), linked to an S-parameter block named S_J that takes into account the behavior of the slotline junction. This block has three ports since the slotline junction can be seen as a 1-to-2 power divider where the output ports have a characteristic impedance Z_r. The ring branches are connected to these ports, and the PIN diode (whose admittance is Y_d) is placed between these two branches, whose lengths are $L_r/4$ and $3L_r/4$, as shown in Fig. 3(a). The S_J of the slotline junction can be derived by performing a circuit analysis of voltages and currents at the discontinuity, as marked in Fig. 2(c). From this analysis, the following relationships are obtained:

$$I_1 = -I_2; \quad I_1 = I_3; \quad V_1 = V_2 - V_3. \tag{1}$$

Assuming the relation between characteristic impedances is $Z_r = Z_s/2$, S_j is derived through the relations of the above voltages and currents to their corresponding power waves [30, Ch. 4]. It is expressed as follows:

$$[S_J] = \begin{pmatrix} 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} & \frac{1}{2} & \frac{1}{2} \\ -\frac{1}{\sqrt{2}} & \frac{1}{2} & \frac{1}{2} \end{pmatrix}. \tag{2}$$

The values of the S_J correspond to those associated with the S-matrix of a classical E-plane divider in waveguide, where the output ports are out of phase. Once the slotline junction matrix is computed, an expression for the reflection coefficient Γ_{IN} of the unit cell with ring configuration can be derived. Considering the power waves (a_n and b_n) of each port of the slotline junction and their associated flow graph [see Fig. 3], Mason's rule is applied (the derivation is in Appendix A) to obtain the following expression:

$$\Gamma_{IN} = \frac{b_1}{a_1} = \frac{\frac{1}{2}\Gamma_2 + \frac{1}{2}\Gamma_3 - \Gamma_2\Gamma_3}{1 - \frac{1}{2}\Gamma_2 - \frac{1}{2}\Gamma_3}, \tag{3}$$

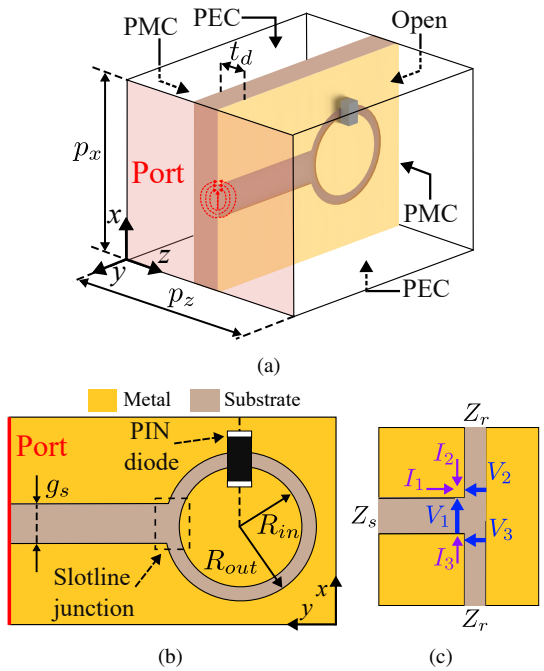

Fig. 2: Ring configuration of the 1-bit slotline unit cell: (a) 3D view, (b) Planar view and, (c) Planar view of the slotline junction. The dimensions (in mm) are: $p_x = p_y = 3$, $g_s = 0.55$, $R_{out} = 0.8$ and, $R_{in} = 0.7$.

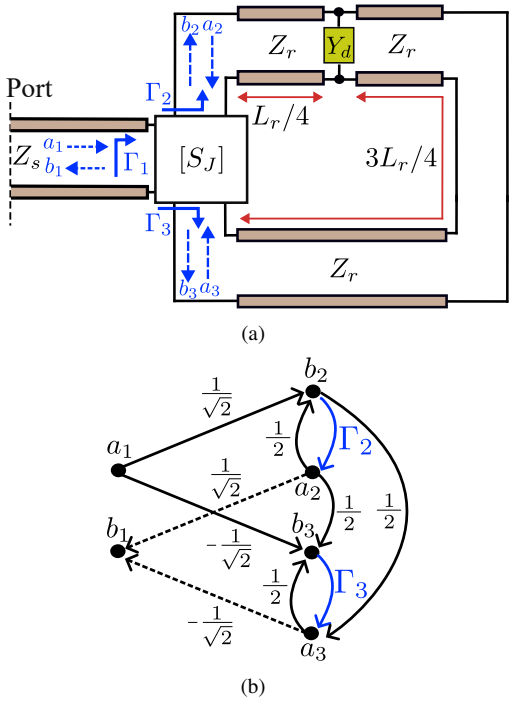

Fig. 3: (a) Circuit model for the slotline unit cell with ring configuration. (b) Flow graph of the involved power waves in the slotline junction.

where $\Gamma_2 = a_2/b_2$ and $\Gamma_3 = a_3/b_3$. Now, the equivalent load of the circuit between the output ports of the slotline junction is derived. Its circuit is constituted by the transmission line of length $L_r/4$, the admittance Y_d, and the other transmission line of length $3L_r/4$. The S-matrix of a shunt admittance is as follows [30, Ch. 4]:

$$[S_d] = \begin{pmatrix} \frac{-y}{2+y} & \frac{2}{2+y} \\ \frac{2}{2+y} & \frac{-y}{2+y} \end{pmatrix}, \tag{4}$$

where $y = Y_d Z_r$. If we consider that $L_r = \lambda_g$, being λ_g the wavelength along the slotline ring, the shunt admittance is sandwiched between a $\lambda_g/4$ and a $3\lambda_g/4$ lines. This is translated to apply the appropriate de-embedding in each side of the shunt admittance. The resulting S-matrix after the de-embedding is the following one:

$$[S_{d,eq}] = \begin{pmatrix} \frac{y}{2+y} & \frac{2}{2+y} \\ \frac{2}{2+y} & \frac{y}{2+y} \end{pmatrix}. \tag{5}$$

This can be converted to an ABCD-matrix that is

$$[ABCD_{d,eq}] = \begin{pmatrix} 1 & Z_r y \\ 0 & 1 \end{pmatrix}. \tag{6}$$

The values of the above matrix indicate that the equivalent load between ports of the slotline junction is a series impedance Z whose expression is

$$Z = Y_d \frac{Z_s^2}{4}. \tag{7}$$

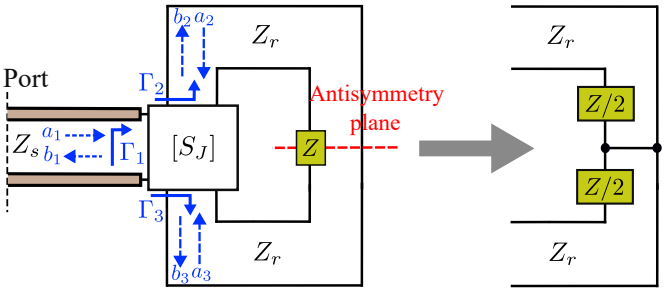

Fig. 4: Circuit model for the slotline unit cell with ring configuration with the equivalent load for the PIN diode and ring branches.

Thus, the equivalent circuit for the slotline ring is the series impedance Z shown in Fig. 4. Nevertheless, this equivalent circuit has an alternative representation due to the out-of-phase behavior at the output ports of the slotline junction. Considering this fact, it has virtually created an antisymmetric plane (like in an odd-mode analysis), as indicated in Fig. 4. This produces an impedance split of Z and consequently, the reflection coefficients can be computed as

$$\Gamma_2 = \Gamma_3 = \frac{\frac{1}{2}Z - Z_r}{\frac{1}{2}Z + Z_r} = \frac{Y_d \frac{Z_s^2}{8} - \frac{1}{2}Z_s}{Y_d \frac{Z_s^2}{8} + \frac{1}{2}Z_s} = \frac{Y_d Z_s - 4}{Y_d Z_s + 4}. \tag{8}$$

Since $\Gamma_2 = \Gamma_3$, this is used in (3) to directly obtain the following equation:

$$\Gamma_{IN} = \frac{\Gamma_2 - \Gamma_2^2}{1 - \Gamma_2} = \Gamma_2. \tag{9}$$

This indicates that the reflection behavior of the slotline unit cell is determined by (8), whose expression depends only on

TABLE III: Reflection coefficients for the classical and ring configurations.

Classical	$\Gamma_{IN}^{ON} = \dfrac{1 - Y_{ON} Z_s}{1 + Y_{ON} Z_s}$	$\Gamma_{IN}^{OFF} = \dfrac{1 - Y_{OFF} Z_s}{1 + Y_{OFF} Z_s}$
Ring	$\Gamma_{IN}^{ON} = \dfrac{\frac{Y_{ON}}{4} Z_s - 1}{\frac{Y_{ON}}{4} Z_s + 1}$	$\Gamma_{IN}^{OFF} = \dfrac{\frac{Y_{OFF}}{4} Z_s - 1}{\frac{Y_{OFF}}{4} Z_s + 1}$

TABLE IV: Reflection coefficients at 40 GHz considering a real PIN diode.

PIN	Classical conf.	Ring conf.
ON	$\Gamma_{IN}^{ON} = 0.932e^{j169.7^o}$	$\Gamma_{IN}^{ON} = 0.776e^{-j40.2^o}$
OFF	$\Gamma_{IN}^{OFF} = 1e^{-j116.3^o}$	$\Gamma_{IN}^{OFF} = 1e^{j136.1^o}$

Y_d and Z_s. For the sake of comparison, Γ_{IN} of the classical configuration (when $L_s = \lambda_g/4$) has been included in Table III together with Γ_{IN} of the ring configuration. The expressions in this table indicate that for the ring, the PIN diode admittance is divided by a factor of 4, which is not the case for the classical configuration. Consequently, this improves the OFF state of the ring configuration because a small Y_{OFF} is required to get a better short circuit. On the contrary, this worsens the ON state because a large Y_{ON} is preferable. For a high operating frequency, the main problem is the OFF state [see Table II], as it is difficult to find a commercial PIN diode with a small enough $C_{d,OFF}$. Table IV is included to help understand this comparison better. It evaluates the expressions of Table III for the case of a commercial PIN diode [32] whose circuit values are found in the caption of Fig. 1. In the case of the classical configuration in Table IV, the ON state provides a reflected phase close to 180º (similar to a short circuit). However, the reflected phase for the OFF state is -116.3º, far from the 0º that would be obtained for an open circuit. In the ring configuration, the ON state produces a reflected phase close to 0º, i.e., the open-circuit behavior is significantly improved. It is important to note that for the ring configuration, the states are reversed compared to the classical ones, as can be found in the equations of Table III. For the OFF state, the short-circuit behavior worsens slightly, but overall, the phase difference is improved, reaching approximately the targeted 180º.

To verify the developed circuit model, a comparison is made in Fig. 5 between the simulated results obtained from the simulations of the unit cell presented in Fig. 2(a) and those obtained using the circuit model. Figs. 5(a)-5(c) show the phase difference performance versus frequency between the two states of the PIN diode in the ring configuration. Fig. 5(a) demonstrates, from 35 GHz to 45 GHz, that in addition to reaching $-180°$ of phase difference at the design center frequency considering a real PIN diode, this desired 1-bit reconfiguration behavior is maintained over a large bandwidth. This means that the analyzed response of the proposed ring configuration is robust across frequency, providing a key improvement over the classical configuration. Moreover, Fig. 5(a) demonstrates how the ring configuration preserves the 1-bit performance over a large bandwidth similar to that obtained if an ideal PIN diode is used. In Figs. 5(b) and 5(c), it is

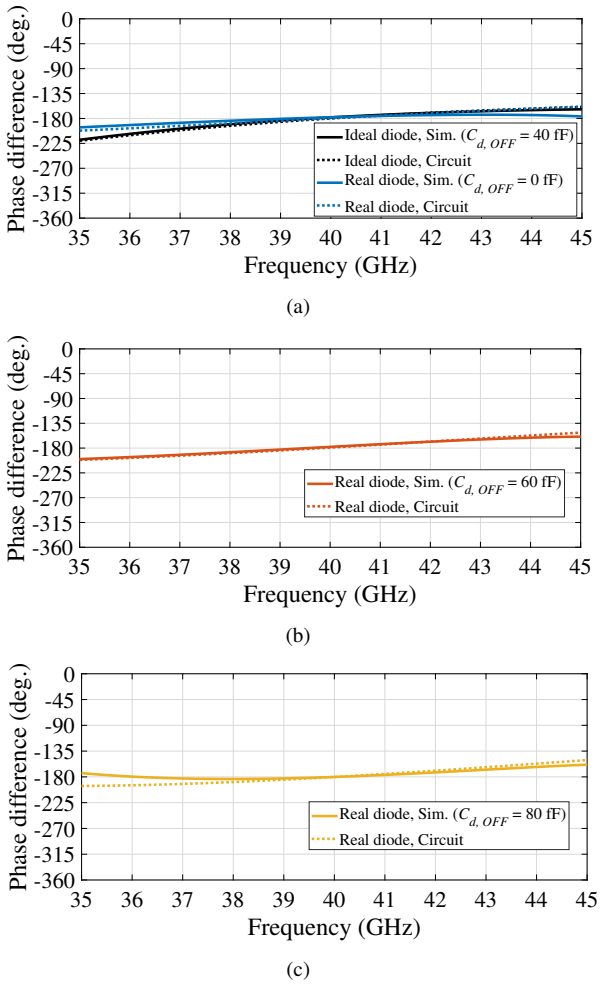

Fig. 5: Reflection phase difference between PIN diode states (ring configuration) when is used: (a) an ideal diode and one whose $C_{d,OFF} = 40$ pF, (b) a diode whose $C_{d,OFF} = 60$ pF and, (c) a diode whose $C_{d,OFF} = 80$ pF. The dimensions (in mm) for L_r in each case are: (a) 2.67 (ideal case) and 4.44 (real case), (b) 3.66, and (c) 3.06.

demonstrated that even for cases where the OFF state is worse (higher value for $C_{d,OFF}$), a phase difference around 180° from 35 GHz to 45 GHz is achieved. This can be accomplished simply by adjusting the ring length L_r. It should be noted the agreement between the circuit model and the simulations. This allows to have a tool to efficiently find the ring dimensions that provide the 1-bit response according to the impedance of the considered PIN diode.

D. Losses in the 1-bit slotline unit cells

This subsection discusses the losses of the 1-bit slotline unit cells presented above. For this purpose, the following lossy materials have been considered: copper ($\sigma = 5.8{\cdot}10^7$ S/m) and loss tangent for the RO4003C of 0.005 at 40 GHz. The series resistance R_d of the PIN diode has also been considered as it is a source of losses. Fig. 6(a) and 6(b) display the reflection losses for both configurations. It is observed that with periodic boundary conditions (PEC-PMC), the ring configuration presents more losses in the ON state compared to the ON state of the classical configuration. This increase

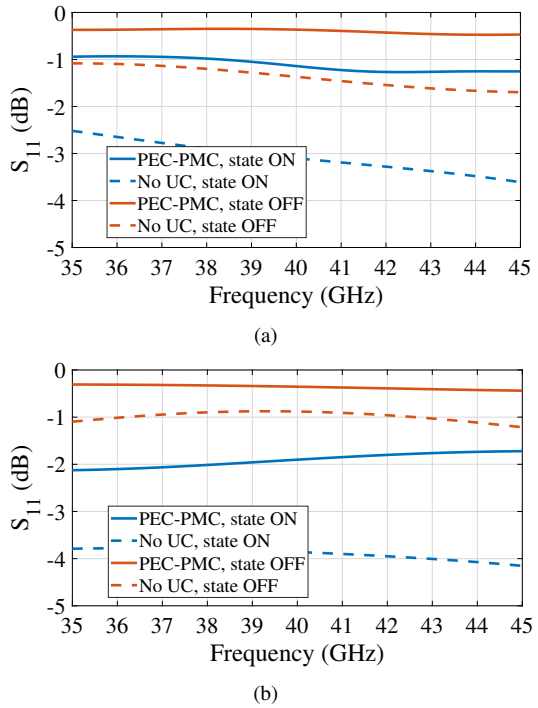

Fig. 6: Reflection coefficient in magnitude for both PIN diode states when it is selected a: (a) Classical configuration and, (b) Ring configuration.

in losses is due to the fact that both configurations have a different reflection mechanism due to their design. This was well predicted by the analysis in section II.C that showed that the ON state (the one responsible for losses) in the ring configuration was degraded [see Table IV]. However, although the ring configuration has more losses, it has the great advantage that the phase difference between states is 180º, which is essential for performing beam-steering. Moreover, in the OFF state of both configurations, there are losses mainly due to the use of dielectrics. In the case that materials with higher losses or a higher value for R_d were considered, the 1-bit reconfiguration bandwidth for the ring configuration would not be compromised.

For the sake of completeness, when no periodic conditions are set around the unit cell, it is also assessed. In that case, open-boundary conditions are set around the unit cell. For that case (named non-UC), the losses increase up to 2.5 dB due to the radiation occurring when a propagating wave is reflected in a slotline discontinuity. When the unit cell is in a periodic environment, this unwanted radiation is mitigated.

III. Experimental Validation and Discussion

A. Reconfigurability

To experimentally validate the reconfigurable performance of the proposed slotline unit cells, a circuit prototype is developed and illustrated in Fig. 7. This prototype implements a double-sided copper board RO4003C with a thickness of 0.508 mm. In this prototype, it is implemented the two slotline unit cell designs (indicated as classic and ring configurations) and a microstrip TRL kit. The TRL kit is employed to remove all undesired measurement effects from connectors and cables in the setup. Fig. 7(a) shows the top view of the prototype in which broadband transitions from coaxial line to microstrip line can also be seen in each of the ports to feed the TRL kit and slotline unit cells. These transitions are necessary to measure the prototype with the vector network analyzer (VNA) R&S-ZVA67, whose measurement ports are 1.85mm coaxial. In combination with these transitions, the end launch connectors (model 91R60918 of Southwest Microwave) are used to facilitate the connection between the prototype and the 1.85mm VNA coaxial cables. Therefore, the designed coaxial to microstrip transition provides a broadband impedance matching from the coaxial port, which is the end-launch connector output, to the microstrip transmission line, which feeds the slotline unit cells. The design of this transition allows a smooth modification of the TEM mode coming from the coaxial end-launch connector to the quasi-TEM mode of the microstrip line. This is due to the inclusion of a tapered transmission line based on a grounded coplanar waveguide where the separation between conductors is increasing [see top layer view in Fig. 7(b)]. The simulated reflection coefficients of both ports ($|S_{11}|$ and $|S_{22}|$) for the described transition is below -16 dB from 35 GHz to 45 GHz.

The reconfigurable slotline unit cells are fed by the microstrip line coming from the above-mentioned coaxial to microstrip transition. This microstrip line ends in a microstrip to slotline transition in order to transmit the incident power to the reconfigurable slotline unit cells. For this purpose, a transition based on the work [34] is designed to the frequency band of interest and with the selected microstrip and slotline dimensions. The layout of these transitions from microstrip to slotline are depicted in Figs. 7(b) and 7(c). Note that the prototype has copper on both sides of the board; the microstrip lines have been implemented on one side [see Fig. 7(a)], while the slotlines have been manufactured on the other side (named bottom layer). The simulated reflection coefficients of the designed microstrip to slotline transitions are around -20 dB at both ports for the selected frequency range. Figs. 7(b) and 7(c) indicate in blue the location of the reference plane where the port is positioned after calibration with the TRL kit. Figs. 7(b) and 7(c) also show the inclusion of several double radial stubs in both slotline and microstrip. These double radial stubs are designed to produce a broadband open circuit in the line (microstrip or slotline) where they are placed. Taking this into account and carefully selecting the lengths L_{sc1}, L_{sc2}, and L_r, it allows to short-circuit the points of interest in the layout of both unit cell configurations. This is necessary to perform proper biasing of the PIN diodes without shorting its terminals in the classical configuration. For the ring configuration, a metallic via has been inserted in the center of the ring, which allows easy inclusion of the biasing from the top layer, as shown in Fig. 7(c). The inclusion of the via has a negligible effect compared to the unit cell configuration without this via. This is a great design advantage over the classical configuration, where two double radial stubs have been needed to avoid a short circuit of the PIN diode terminals [see Fig. 7(b)]. The PIN diode used for both reconfigurable slotline unit cells is the MA4AGP907 [32].

Figs. 8 and 9 show the simulated and measured results in

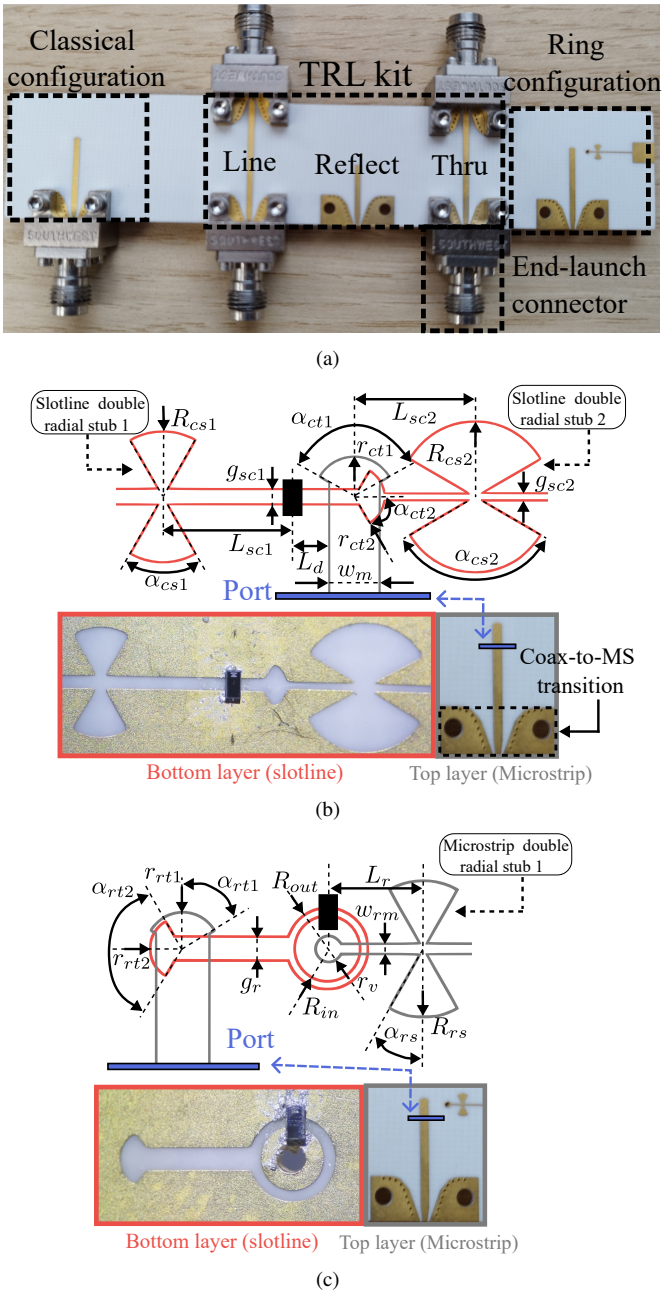

Fig. 7: Circuit prototype of the reconfigurable slotline unit cells: (a) Top view, (b) Top and bottom views of the classical configuration along with its layout and, (c) Top and bottom views of the ring configuration along with its layout. The dimensions (in mm) are: $R_{cs1} = 1.3$, $L_{sc1} = 3.3$, $L_d = 0.7$, $g_{sc1} = 0.3$, $w_m = 1$, $r_{ct1} = 0.8$, $r_{ct2} = 0.6$, $L_{sc2} = 2.4$, $R_{cs2} = 1.5$, $g_{sc2} = 0.14$, $r_{rt1} = 0.7$, $r_{rt2} = 0.6$, $g_r = 0.45$, $R_{out} = 0.775$, $R_{in} = 0.625$, $w_{rm} = 0.2$, $L_r = 1.8$, $R_{rs} = 1.3$, $r_v = 0.3$, $\alpha_{cs1} = \alpha_{ct2} = \alpha_{rt1} = 60$º, $\alpha_{ct1} = \alpha_{cs2} = \alpha_{rt2} = 120$º and, $\alpha_{rs} = 30$º.

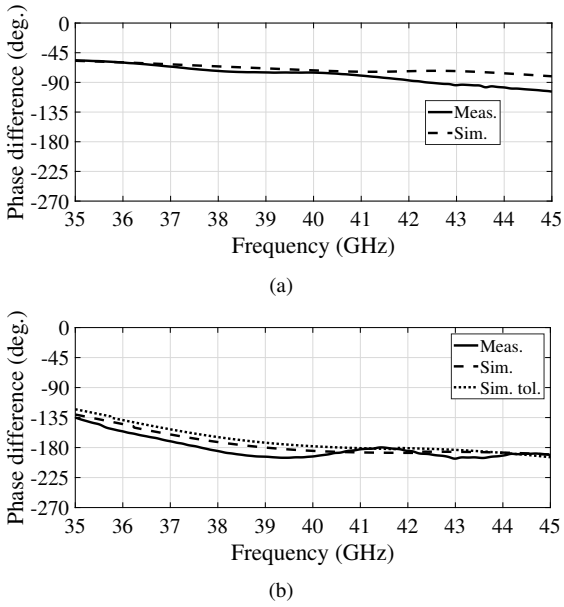

Fig. 8: Simulated and measured results for the phase performance in the: (a) Classical configuration and, (b) Ring configuration.

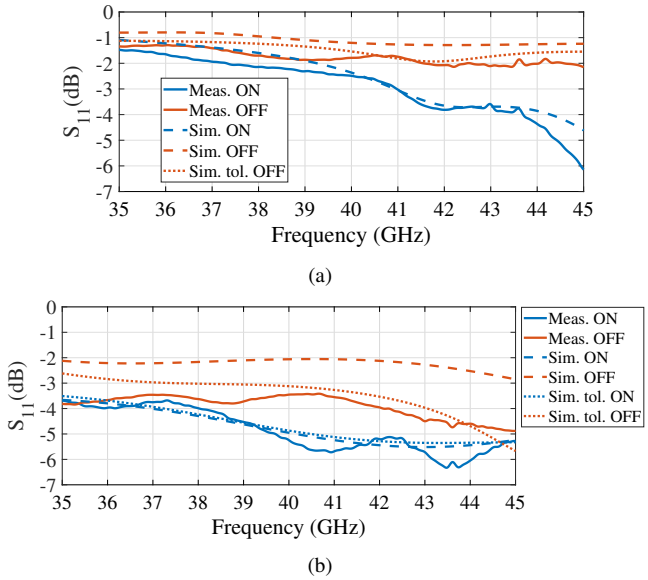

Fig. 9: Simulated and measured results for the magnitude performance in the: (a) Classical configuration and, (b) Ring configuration.

phase and magnitude for both slotline unit cell configurations, respectively. There is a good agreement between simulations and measurements demonstrating the capability of the ring configuration to achieve a $-180° \pm 20°$ phase difference from 36.3 GHz to 45 GHz, which represents a 21.4% relative bandwidth. For the classical configuration, the PIN diode is placed at $\lambda_s/4$ regarding the position of a short circuit created by a double radial stub, this is the value of L_{sc1}. This corresponds to the real diode case in Fig. 1(c). The measured results show about 75º of phase difference at 40 GHz, revealing the non-idealities of the PIN diode states in this frequency range. Indeed, Fig. 8 also demonstrates that the ring configuration is able to provide 1-bit reconfiguration while the classical configuration is not. The 180º phase difference is essential to allow effective reconfiguration of the reflected wave by the device (reflectarray or RIS) hosting the unit cell.

Regarding the losses in reflection presented in Fig. 9, the ring configuration presents a higher level, which was expected. It must be taken into account that the experimental validation is on a PCB circuit and thus, the unit cells have an open boundary conditions. As explained in section II.D, this

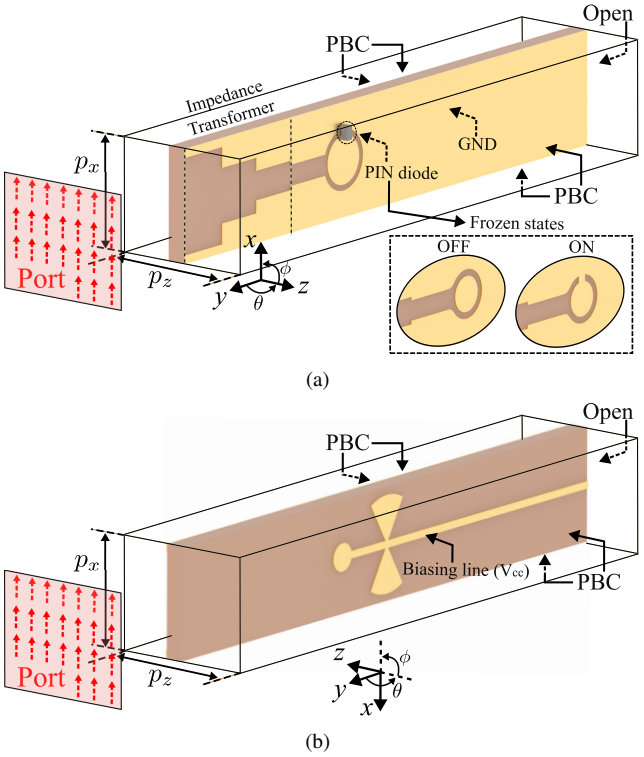

Fig. 10: 3-D views of the reconfigurable slotline unit cell with ring configuration and its frozen states. (a) Front side: impedance transformer and 1-bit slotline ring layout. (b) Back side: biasing circuit layout. The dimensions are $p_x = p_y = 3$ mm. PBC and GND stand for Periodic Boundary Condition and Ground, respectively.

situation does not mitigate the radiation losses as do periodic boundary conditions, which are going to be the implementation environment for the proposed unit cells. It is verified that the simulated unit cell performances are consistent with the measurements both in phase and magnitude as can be checked in Fig. 8 and Fig. 9, respectively. In addition, certain tolerances confirmed with simulations have been observed such as, for example, the presence of a series resistor in the OFF state (also found in [25]) and a slight displacement of the diode position in the ring configuration. Fig. 8(b) also includes the mentioned tolerances and they do not cause an alteration of the 1-bit behavior provided by the ring configuration. It should be pointed out that noting the good agreement between simulated and measured results, when the unit cell is included in a periodic environment, the losses will be reduced, as demonstrated in Fig. 6.

B. Complete array

In this section, in order to complete the EM assessment of the slotline unit cell with ring configuration, the proposed slotline unit cell is tested in periodic and quasi-periodic environments. For this purpose, Fig. 10 presents the proposed slotline unit cell. To develop this slotline unit cell design (that is) well-suited for feeding by a plane wave coming from free space (RIS application), the following design process has been followed:

- First, the design relies on boundary conditions and excitation shown in Fig. 2(a). At this step, the main dimensions of the slotline ring are tuned to obtain, in the desired frequency band, the phase difference around 180º.
- Second, a broadband impedance transformer has to be designed and placed before the unit cell designed in the previous step. For this, we consider a three-section impedance transformer following the details found in [35].
- Third, the unit cell design of the first step is combined with the broadband impedance transformer of the second step resulting in the RIS unit cell illustrated in Fig. 10(a).

The broadband impedance transformer reduces reflections at the interface between the free space and the slotline unit cell. This reduction of reflections in unit cells is desired to preserve phase linearity over the frequency [36]. In addition, in this slotline unit cell with PIN diode, the biasing circuit has been included on the backside of the board (the same as displayed in Fig. 7(c)) to take into account its effect in the EM simulations. The distances between unit cells, p_x and p_z, correspond to electrical wavelength values of $0.35\lambda_L$ and $0.45\lambda_H$ for the minimum and maximum frequency of the considered operating bandwidth. The length along the y-axis (longitudinal dimension) can be bigger than the wavelength without compromising the radiation performance of the RIS since it is a 3-D unit cell. Fig. 10(b) shows the back side of the view displayed in Fig. 10(a). This side of the proposed slotline unit cell includes the biasing circuit for the PIN diode. The design of this circuit is the same as the one used in Fig. 7(c), which is mainly composed of a microstrip double radial stub and a via connecting the central metal part of the slotline ring with the biasing circuit. The biasing line sets the bias voltage of the PIN diode while the ground of the PIN diode is the metal part that covers almost the entire unit cell [see Fig. 10(a)]. It is important to note that the presence of the biasing line has a negligible effect on the performance of the reconfigurable unit cell. For the sake of reducing complexity in the experimental assessment, Fig. 10(a) also illustrates the static version of the proposed unit cell design where the PIN diode has been replaced by an ideal switch. The ON state is produced by means of a metallic strip with the same size as the PIN diode and, the OFF state by the absence of this metallic strip. The reconfigurable slotline unit cell will be referred as RIS UC, while its static version will be named as frozen RIS UC. The dimension of the slotline ring of the frozen RIS UC is slightly different in comparison with the one in RIS UC to achieve equivalent performance in the same frequency range. Coming back to Fig. 5(a), where the phase behavior of the unit cell with ring configuration is compared for a real and an ideal PIN diode, it is observed that similar phase performance is achieved only by modifying L_r [see caption of Fig. 5]. To demonstrate this claim, EM simulations of the slotline unit cells presented in Fig. 10 have been performed. Periodic boundary conditions (PBCs) and a Floquet port, where the electric field is in the x-direction, have been considered. The simulated results, in magnitude and phase for each of the states of the RIS UC and frozen RIS UC, are displayed in Fig. 11. In Figs. 11(a) and 11(b), the results are computed in a normal incidence situation ($\theta = 0^{\text{o}}$) while the results in Figs. 11(c)

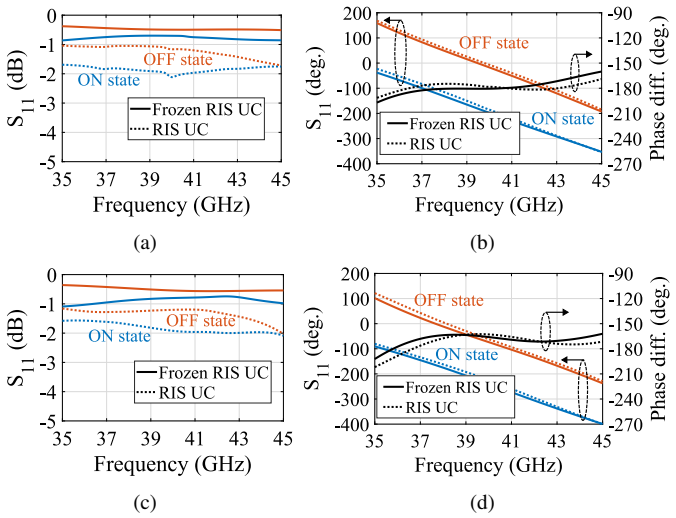

Fig. 11: Performance comparison between the RIS UC and Frozen RIS UC. Simulated results in magnitude for (a) normal incidence and (c) oblique incidence with $\theta = 30^{\text{o}}$. Simulated results in phase for (b) normal incidence and (d) oblique incidence with $\theta = 30^{\text{o}}$.

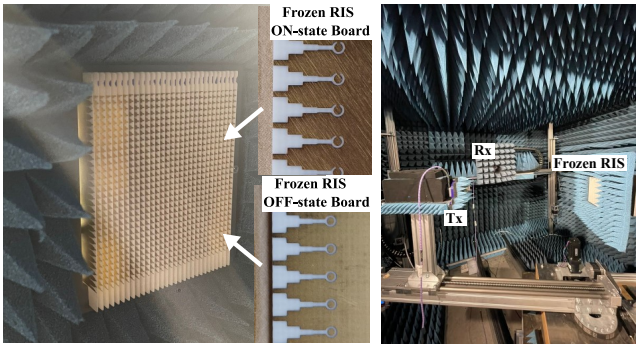

Fig. 12: (a) Frozen RIS prototype and its forming boards and, (b) Measurement setup where Tx and Rx stand for the transmitting and receiving standard 20-dBi horn antennas.

and 11(d) are obtained from an oblique incidence situation, where $\theta = 30^{\text{o}}$. It is important to mention that in the OFF state of the PIN diode, the series resistance found in the measured results of Fig. 9 has been also included in the simulations. The comparison between the two slotline unit cells reveals a great similarity in the reflection performance (magnitude and phase) at both normal and oblique incidence. Regarding the phase behavior, a phase difference between states of $-180^{\text{o}} \pm 20^{\text{o}}$ is approximately preserved in both normal and oblique incidence from 35 GHz to 45 GHz. Corresponding to the performance in magnitude, on the one hand, the frozen RIS UC produces losses of less than 1 dB for both states in both incidence situations. On the other hand, for the RIS UC, these losses increase by 1 dB on average, not reaching losses greater than 2 dB in the considered frequency range. The reflection losses are mainly produced by the non-zero value of the resistance R_d present in practice in both states of the PIN diode. Losses due to materials (metal and dielectric) have a minor contribution. Therefore, to improve the observed losses for the RIS UC, the most direct way is to decrease the resistance value of the PIN diode. The frozen RIS UC, in its two states, produces equivalent phase performance to the RIS UC at both normal and oblique incidence. The behavior in magnitude is also equivalent except for an increase in losses, which is expected due to the non-zero resistance of the PIN diode states.

The prototype for experimental validation and the measurement setup are shown in Figs. 12(a) and 12(b), respectively. The prototype for the frozen RIS is composed of the arrangement of RO4003C boards with a thickness of 0.508 mm, where each board implements 30 frozen RIS UCs. In other words, the board is formed by the concatenation in x-direction [see axes in Fig. 10] of frozen RIS UCs. Therefore, the largest dimension of the board is 9 cm. If we take a closer look at Fig. 12(a), we see that all frozen RIS UCs of one given board are the same, i.e., they are either in the ON state or in the OFF state. In our case, following the boundary conditions shown in Fig. 10, the boards are placed in the z-direction with a separation between them of p_z. To maintain this separation, a 3-D printed plastic support has been used (placed at the back of the prototype) where all the frozen RIS boards are inserted. The total number of layers composing the prototype is also 30. As the boards which compose frozen RIS are not fixed and can be exchanged manually, the phase (or bit) distribution can be easily rearranged. This rearrangement is performed in the YZ plane so the beam steering of the anomalous reflection is in the same plane.

Firstly, we characterized a frozen RIS panel where all unit cells are in ON state and another one where they are all in OFF state. The corresponding reflection performance are given in Fig. 13. The magnitude and phase of the simulated and measured results are shown in Figs. 13(a) and 13(b), respectively. Additionally, measurements have been carried out for normal and oblique incidence. It can be seen that for the whole frequency band examined and in both incidence situations, the reflection losses are not more than 2 dB for both states. This represents an extra loss of about 1 dB in average compared to the simulated results. The causes of this may be due to the tolerances in the measurement setup and prototype assembly where the magnitude measurement is more sensitive. In relation to the performance of the phase difference between states shown in Fig. 13(b), very similar results to those obtained in simulation are obtained in both normal and oblique incidence. Although there are some differences such as a displacement of the central value of the phase difference, in both incidence cases, the planar response of the phase difference at the target frequency range is maintained with a tolerance of approximately $\pm$ 20°.

Finally, the capability of the frozen RIS to perform broadband anomalous reflections using the 1-bit phase distribution has also been evaluated. This measure corresponds to the evaluation of the proposed slotline unit cell in a quasi-periodic environment. For this purpose, both a normal incidence with an output angle of $\theta_o = 25^{\text{o}}$ and the opposite one, i.e., incidence in $\theta_i = 25^{\text{o}}$ and output angle at $\theta_o = 0^{\text{o}}$, have been considered. The simulated and measured normalized radiation patterns at several frequencies are displayed in Fig. 14 for normal incidence and in Fig. 15 for oblique incidence. The bit distribution

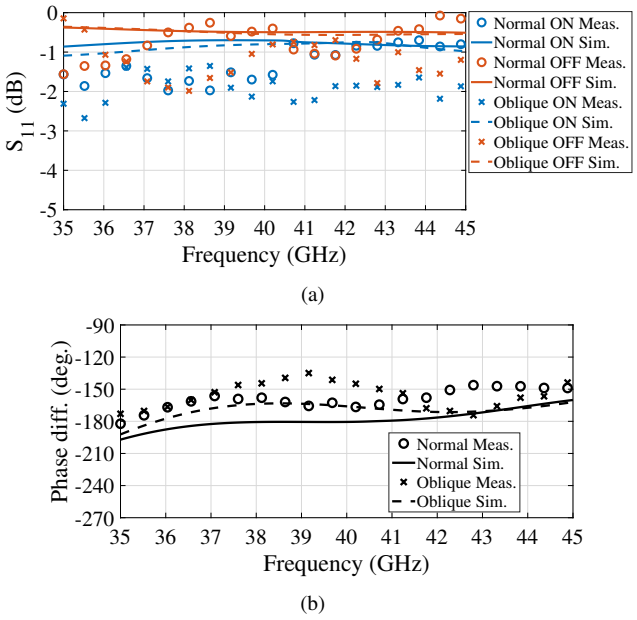

Fig. 13: Measured and simulated performance of the frozen RIS UC at normal and oblique incidence ($\theta = 30^{o}$): (a) in magnitude and (c) in phase.

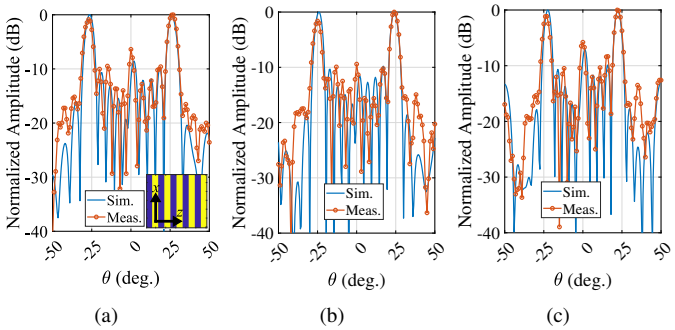

Fig. 14: Simulated and measured normalized radiation patterns in the YZ plane ($\phi = 0^{o}$) of the frozen RIS: (a) at 37 GHz, (b) 40 GHz and, (c) 43 GHz. Normal incidence is considered, i.e., $\theta_i = 0^{o}$. The inset in (a) indicates the employed bit distribution where yellow and blue represent the frozen RIS UC in OFF and ON state, respectively.

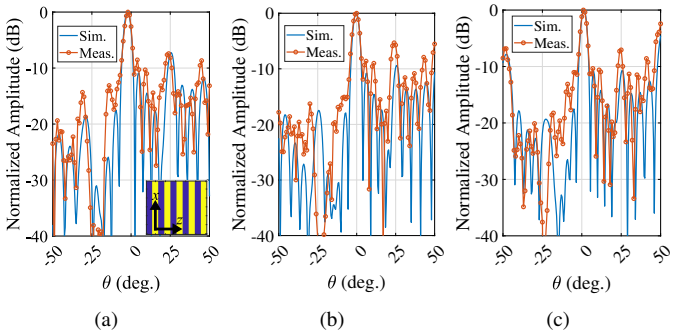

Fig. 15: Simulated and measured normalized radiation patterns in the YZ plane ($\phi = 0^{o}$) of the frozen RIS: (a) at 37 GHz, (b) 40 GHz and, (c) 43 GHz. Oblique incidence is considered, i.e., $\theta_i = 25^{o}$. The inset in (a) indicates the employed bit distribution where yellow and blue represent the frozen RIS UC in OFF and ON state, respectively.

used is shown in the inset of Figs. 14(a) and 15(a), where yellow and blue represent the frozen RIS UC in OFF and ON state, respectively. The good agreement between simulated and measured results is observed for both assessed situations in a wide frequency range. In fact, both the main beam and the secondary lobes are quite similar to those obtained in simulations, which reinforces that the unit cells have an EM behavior quite close to those obtained in simulation. It is worth mentioning in Fig. 14 that by using a plane wave excitation in combination with a 1-bit configuration, it is natural the appearance of a quantization lobe which is symmetrical to the desired one [21]. Note that obtaining a good anomalous reflection in complementary incidence situations demonstrates the reciprocity of the frozen RIS and its ability to support bidirectional communications [37]. Furthermore, the results for the frozen RIS in a periodic or quasi-periodic environment are equivalent to those of the RIS but with an increase in reflection losses in average of 1 dB for both states [see Figs. 11(a) and 11(c)]. Therefore, in the implementation of the RIS with PIN diodes, it is expected losses of 2 dB (taking into account both UC states) and maximum losses of 3.5 dB.

C. Frequency rescaling, comparison and discussion

In this work, we have chosen the center frequency of 40 GHz since, thanks to the broadband 1-bit performance of the proposed RIS unit cell, it covers the n259 and n260 bands. However, our unit cell design also supports easy frequency rescaling without losing the great benefit of the 1-bit reconfiguration bandwidth. To demonstrate this fact, we have considered two cases of redesign with higher frequencies. The first with a center frequency at 60 GHz and the second with a center frequency at 72.5 GHz. It should be noted that the R_d, L_d and C_d values of the PIN diode circuit model [see Fig. 1(b)] have been maintained. The redesign process follows the RIS unit cell design steps detailed at the beginning of section III.B. The values of the most relevant dimensions of the RIS unit cell for each case are indicated in the caption of Fig. 16. It can be seen that the reflection losses for both cases are no more than approximately 4 dB in both analyzed frequency ranges. In both redesign cases we have considered for the OFF state the series resistor R_d. The point of main interest in Fig. 16 is that in both cases, the phase difference of $-180^{o} \pm 20^{o}$ is preserved. This means that the relative bandwidths for the 1-bit reconfiguration are 33% and 20.69% for the 60 GHz and 72.5 GHz case, respectively.

A comparison of the performance between the proposed slotline unit cell with ring configuration and previous reflective PIN diode-based unit cells is presented in Table V. Our proposed slotline unit cell fills the gap about this type of reflective unit cells offering a relative bandwidth greater than 20% where the achieved phase difference is $180^{o} \pm 20^{o}$. Only the RIS UC in [22] achieves a relative bandwidth comparable to the one proposed but in a frequency band below 30 GHz where the PIN diode performs better. Moreover, the results presented on the RIS UC in [22] are only simulated. The RIS UC design proposed in this work achieves a 1-bit performance with a single PIN diode up to 45 GHz [see Fig. 8(b)]. As far as the authors are aware, the use of a single PIN diode for 1-bit broadband reconfigurability in this millimeter-wave

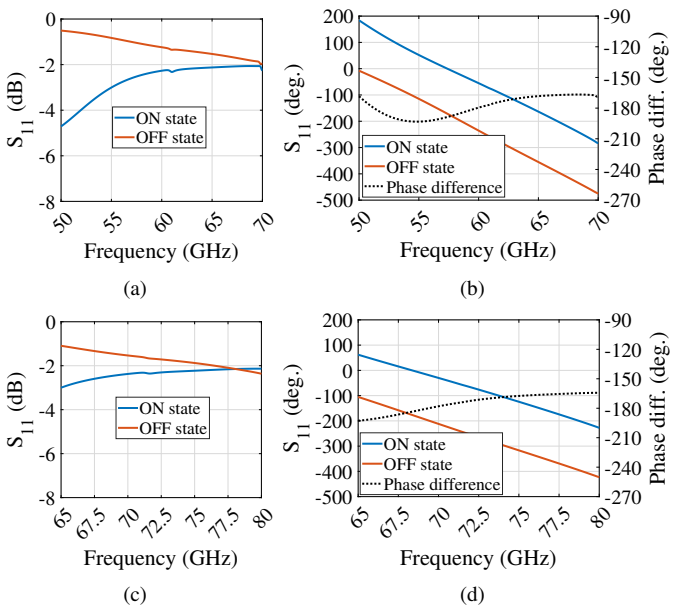

Fig. 16: Performance of the redesigned RIS UCs at 60 GHz and at 72.5 GHz. For the 60 GHz redesign, simulated results (a) in magnitude and (b) in phase. For the 72.5 GHz redesign, simulated results (c) in magnitude and (d) in phase. Dimensions in mm for 60 GHz redesign: $R_{out} = 0.375$, $R_{in} = 0.225$, $g_s = 0.5$, $t_d = 0.305$, $p_x = p_z = 2.1$. Dimensions in mm for 72.5 GHz redesign: $R_{out} = 0.32$, $R_{in} = 0.195$, $g_s = 0.4$, $t_d = 0.305$, $p_x = p_z = 1.8$.

frequency band has not been previously reported. Additionally, its design has been shown to be readily scalable to higher frequencies while preserving the 1-bit reconfiguration bandwidth improvement. Regarding the maximum losses, which refer to the highest losses reached in one of the reconfigurable unit cell states in its operating frequency band, our unit cell achieves an acceptable level of losses regarding other works in the literature. It is important to highlight that the maximum losses have been estimated in a realistic manner by combining measured (frozen RIS UC and RIS UC in circuit prototype) and simulated results. The losses produced by the proposed RIS UC is one of the points for improvement in the future as well as its extension to a larger number of bits (or reflected phases). The frequency band between 37 GHz and 43.5 GHz will have great potential for future wireless communications since in these frequencies are located the n259 and n260 bands for 5G FR2. In addition and with great importance, the phase reconfiguration in the unit cell is produced using a single PIN diode, which saves cost and reduces complexity in the biasing circuit of the prototype.

IV. Conclusion

In this paper, we introduced a novel slotline unit cell design featuring a slotline ring configuration to achieve 180º phase shift (1-bit reconfiguration) in reflection over a broad bandwidth at millimeter-wave frequencies. This design addresses the limitations of commercial PIN diodes at these frequencies, mainly mitigating the bandwidth degradation for the 1-bit reconfiguration when frequency increases. By comparing our proposed ring configuration to a classical single-slotline unit cell with a single PIN diode, we demonstrated the superior performance of the ring-based approach in achieving robust and wideband 1-bit reconfiguration.

TABLE V: Comparison with other PIN diode-based unit cells in the literature that produce reflection phase reconfigurability

Ref.	Center Freq.	Relative Bandwidth*	Number of PIN diodes	Polarization	Max. losses (dB)
[19]	28 GHz	7.1%	1 (1-bit)	Single linear	1.9★
[21]	28.5 GHz	7%	2 (1-bit)	Dual linear	6
[22]	26.6 GHz	29.3%	1 (1-bit)	Single linear	2.8★
[23]	29 GHz	n. a.	2 (2-bit)	Single linear	2.1★
[24]	60.25 GHz	0.72%	1 (1-bit)	Single linear	5.3
[25]	72.8 GHz	6.86%	2 (1-bit)	Single linear†	6.2
This work	**40**	**21.4%**	**1 (1-bit)**	**Single linear**	**3.5‡**

* Bandwidth where the phase difference is 180º ± 20º.
★ Simulated results.
† It is produced a polarization conversion.
‡ Considering the measured results of the frozen RIS UC in addition to the losses for the PIN diode computed in simulation.

Our in-depth analysis revealed that the classical configuration struggles to obtain broadband performance above 30 GHz due to increasing imperfections in the OFF state of the PIN diode. In contrast, the ring configuration overcomes these limitations, providing a high-tolerance, low-complexity solution that ensures stable EM performance. Circuit analysis has been developed to show the valuable physical insights of the mechanism behind the ring configuration's success. The agreement between circuit models and full-wave simulations underscores the accuracy and utility of our proposed model as a design tool.

Experimental validation further confirmed the advantages of the ring configuration. Prototypes of both configurations were fabricated and measured, with the ring configuration demonstrating a 1-bit performance from 36.3 GHz to 45 GHz, achieving a reflection phase difference of 180º ± 20º (21.4% relative bandwidth). In comparison, the classical configuration produced only 75º of phase difference at 40 GHz. Additionally, the ring configuration simplifies the integration of the PIN diode's biasing circuit into the unit cell structure, enhancing practicality.

Finally, measurements in both periodic and quasi-periodic environments confirmed the capability of the ring configuration to achieve consistent 1-bit reconfiguration across the target millimeter-wave frequency band. Additionally, the proposed unit cell design is highly versatile and can be rescaled in frequency without losing its demonstrated broadband performance, making it adaptable for other frequency bands. The proposed reconfigurable slotline unit cell based on the ring configuration represents a significant step forward in enabling wideband reconfigurable intelligent surfaces (RIS) and reflectarrays at frequencies beyond 30 GHz, while its

ability to be easily rescaled in frequency extends its potential to a wide range of applications in next-generation wireless communication systems.

APPENDIX A

Considering the flowgraph in Fig. 3(b), the associated loops and paths are given below:

- First-order loops:

$$[a_2,b_2] = \frac{1}{2}\Gamma_2$$

$$[a_3,b_3] = \frac{1}{2}\Gamma_3$$

$$[a_2,b_3,a_3,b_2] = \frac{1}{4}\Gamma_2\Gamma_3.$$

- Second-order loops:

$$[a_2,b_2][a_3,b_3] = \frac{1}{4}\Gamma_2\Gamma_3.$$

- Possible paths between a_1 and b_1:

$$[a_1,b_2,a_2,b_1] = \frac{1}{2}\Gamma_2.$$

$$[a_1,b_3,a_3,b_1] = \frac{1}{2}\Gamma_3.$$

$$[a_1,b_2,a_2,b_3,a_3,b_1] = -\frac{1}{4}\Gamma_2\Gamma_3.$$

$$[a_1,b_3,a_3,b_2,a_2,b_1] = -\frac{1}{4}\Gamma_2\Gamma_3.$$

From the Mason's rule, we arrive to the general expression of the input reflection coefficient:

$$\Gamma_{IN} = \frac{b_1}{a_1} = \frac{\frac{1}{2}\Gamma_2(1-\frac{1}{2}\Gamma_3) + \frac{1}{2}\Gamma_3(1-\frac{1}{2}\Gamma_2) - \frac{1}{2}\Gamma_2\Gamma_3}{1-(\frac{1}{2}\Gamma_2 + \frac{1}{2}\Gamma_3 + \frac{1}{4}\Gamma_2\Gamma_3) + \frac{1}{4}\Gamma_2\Gamma_3}, \tag{10}$$

which simplies to expression in (3).

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