Frequency locked loop architecture for phase noise reduction in wideband low-noise microwave oscillators

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Abstract: A frequency locked loop (FLL) for phase noise reduction of wideband voltage controlled oscillators is proposed. The key building block of the system is a low noise (−160 dBV/Hz) and high sensitivity (22 V/GHz) delay line frequency discriminator with 5–8 GHz coverage, which makes use of a high performance multilayer hybrid. The authors derive closed-form, universal design equations for the maximum noise reduction and stability of the FLL circuitry. Application of the proposed technique to a state-of-the-art voltage controlled oscillator operating in the 5–8 GHz band yields a phase noise reduction of 8–10 dB at 100 kHz and 5 dB at 1 MHz off the carrier, which shows the results are in good agreement with the simulated results; so phase noise better than −107 dBc/Hz at 100 kHz and better than −123.5 dBc/Hz at 1 MHz is obtained.

1 Introduction

Nowadays, efficient and robust modulation techniques are demanded in order to reach the high rate data transmission requirements of current radiofrequency standards. Orthogonal frequency division modulation is a widely used modulation technique in wireless communications because of its good performance against noise and multipath effects [1], but it is quite sensitive to local oscillators phase noise [2–5]. In fact, a system with a low phase noise leads to a better bit-error rate in the receiver [1–3]. Consequently, transceivers that make use of these modulation techniques require frequency synthesisers with increasingly low phase noise to avoid leakage of intense adjacent channel interferers due to mixing with oscillator phase noise sidebands [6, 7]; moreover, if referring to synthesisers in metrology and measurement equipment, the specifications for closer frequency channel spacing and higher adjacent channel interference levels are more demanding.

The most used architecture of wideband microwave synthesisers is based on phase locked loop (PLL), which generates stable radiofrequency signals with low phase noise. The core of these PLLs is a voltage controlled oscillator (VCO). Extensive literatures for integrated synthesisers based on PLL can be found in [8, 9]. In PLL synthesisers, phase noise is divided into two different regions. A first region, for low frequency offsets, where phase noise is mainly due to reference oscillator, the phase comparator and the dividers, and a second region, for large frequency offsets, where the VCO phase noise predominates [10]. One of the most important issues in PLL design is to establish its loop filter (LF) parameters. Loop bandwidth is the most critical design parameter, and it is usually selected as a trade-off between lock time, spur level and phase noise [11]. In a relaxed lock-time requirement scenario (as is the case when using a VCO pretuning strategy [12]), the loop bandwidth is usually set at the frequency at which the noise contributions from the VCO equals that from the phase comparator, as this value minimises the total PLL phase noise [11]. This crossing point is in the order of a few hundreds of kHz for typical PLLs operating at GHz frequencies. Selecting a loop bandwidth higher than this value has a detrimental effect on spur level and phase noise, while selecting a lower value improves spur level, but degrades phase noise. Therefore having a lower phase noise VCO enables to reduce loop bandwidth, thus simultaneously reducing total PLL phase noise and spur level.

A possibility to reduce VCO phase noise is to use a VCO inside a frequency locked loop (FLL). Even though FLLs have been previously proposed to reduce the VCO phase noise [12] and improve the linearity of VCOs [13, 14], our approach clearly outperforms the previously reported results. In fact, our solution makes use of a very low noise circuitry, enabling phase noise reduction even in the state-of-the-art low phase noise VCO [15–17]. On the other hand, the proposed FLL feedback circuitry makes direct frequency detection without frequency downconvertion, so the loop delay is decreased, improving the stability of the system. Our design does not aim at an integrated solution, but focuses on offering a convenient way to upgrade the existing frequency synthesisers, used in test and measurement instrumentation, to fulfil stringent noise requirements established by aforementioned standards.

Making use of new closed-form design equations, derived in this work, a FLL has been designed to reduce the phase noise of a high frequency and wideband (5–8 GHz) VCOs up to carrier frequency offsets of 1 MHz. The main building block of the FLL is a wide bandwidth (5–8 GHz) and low noise (−160 dBV/Hz) delay line frequency discriminator (FD) with a sensitivity of 22 V/GHz, which makes use of a previously designed high performance ultra-wideband 90° hybrid [18]. As will be seen in the Section 3.2, with the proposed technique the VCO phase noise level of −104 dBc/Hz can be moved from the original 200 kHz to a new value of 65 kHz off the carrier. Used inside a typical PLL, this will allow for a ÷3 loop bandwidth reduction that will be accomplished by a spur level improvement of $20 \cdot \log(3) = 9.5$ dB for frequencies out of the loop bandwidth and a total phase noise reduction of 5–10 dB for frequencies comprised between the PLL bandwidth and 1 MHz.

This paper is organised as follows: In Section 2, the FLL architecture is analysed as a system and design equations are deduced. A quantitative design for wideband VCO phase noise reduction is carried out using these equations. In Section 3, we present the design and measurements of the delay line FD. In Section 4, we discuss simulated and measured results of the complete FLL prototype. Finally, conclusions are drawn.

2 FLL architecture and design equations

2.1 FLL architecture

The architecture of the proposed FLL is shown in Fig. 1. It consists of five major blocks: (i) the first-order low-pass LF with cutoff frequency ω_{LF} (rad/s); (ii) the VCO, with a sensitivity K_{VCO} (Hz/V); (iii) the FD, also called frequency-to-voltage converter [13], with a sensitivity K_{FD} (V/Hz), converting the VCO output frequency to a voltage, v_{FD}, that is, $v_{FD} = K_{FD} \times f_{out}$; (iv) the delay block, which accounts for the total delay of τ_T (seconds) of all elements in the loop excluding the LF and (v) the adder.

Instantaneous frequency deviations at the VCO output (produced by VCO phase noise) are detected by the FD, whose output voltage (v_{FD}) is proportional to the input frequency (f_{out}). This voltage is subtracted from the input reference voltage (v_r), in order to compensate the oscillator frequency fluctuations. To avoid loop instability, the output signal from de adder is low-pass filtered in the LF.

2.2 Phase noise reduction

As seen in Fig. 1, a noise input $\overline{n_{in}^2}$, including two noise contributions $\overline{n_{VCO}^2}$ and $\overline{n_{ext}^2}$, respectively, accounting for the noise internal and external to the VCO, have been considered for the analysis. Both of them have been referred to the VCO input and thus are measured in V^2/Hz. The internal contribution is set by the VCO and can be directly obtained from its specifications as

$$\overline{n_{VCO}^2}(f) = \frac{S_{\phi VCO}(f) f^2}{|K_{VCO}|^2} \tag{1}$$

where $S_{\phi VCO}(f)$ is the VCO phase noise spectrum and is related to the oscillator single sideband phase noise, $\mathscr{L}(f)$, for a frequency f off the carrier as $S_{\phi VCO}(f) = 2\mathscr{L}(f)$ [7, p. 5]. The external contribution depends on the FD and FLL accompanying circuitry (except the VCO itself). The external noise to VCO noise ratio, η_n, can be defined as

$$\eta_n(f) = \sqrt{\frac{\overline{n_{ext}^2}(f)}{\overline{n_{VCO}^2}(f)}} \tag{2}$$

which measures the noise introduced by FLL circuitry in terms of the VCO phase noise.

Referring to Fig. 1, the loop noise transfer function, from the noise input ($\overline{n_{in}^2}$) to the frequency output (f_{out}), can be written as

$$H_N(s) = \frac{F_{out}(s)}{\sqrt{\overline{n_{in}^2}(s)}} = \frac{K_{VCO}(s + \omega_{LF})}{s + \omega_{LF}(1 + K_{VCO}K_{FD}e^{-s\tau_T})} \tag{3}$$

But, the loop delay in (3) does not affect the total noise reduction inside the FLL bandwidth if $|s\tau_T| \ll 1$, so the loop noise transfer function can be reduced to

$$H_N(s) = K_{VCO}\frac{s + \omega_{LF}}{s + \omega_{FLL}} \tag{4}$$

where ω_{FLL} is the FLL loop bandwidth (rad/s) which is given by $\omega_{FLL} = \omega_{LF}(1 + G_{OL})$ and G_{OL} is the DC open loop gain, defined as $G_{OL} = K_{VCO} \cdot K_{FD}$ (V/V). In most practical situations G_{OL} is much greater than unity so the FLL loop bandwidth can be approximated as $\omega_{FLL} \simeq \omega_{LF}G_{OL}$.

The FLL noise power reduction, R_T^2, is then defined as the ratio between the output noise power of the free running VCO and the total output noise power of the complete FLL. It can be easily calculated, from (2) and (4), as

$$R_T^2 = \frac{1}{1 + \eta_n^2}\left|\frac{s + \omega_{FLL}}{s + \omega_{LF}}\right|^2 \tag{5}$$

The rightmost term in (5) is the ideal FLL noise reduction, that is, the one that would be achieved with noiseless FLL external circuitry, whereas the other term accounts for the FLL noise reduction penalty because of noisy circuitry. Notice that (5) establishes ω_{FLL} as the maximum frequency for which the FLL is still capable of achieving noise reduction in the ideal situation $\eta_n = 0$.

2.3 Stability criterion

The noise reduction capability of the loop is limited by its stability. As the FLL is a simple feedback system, we can use the Bode criterion to obtain a stability condition. The

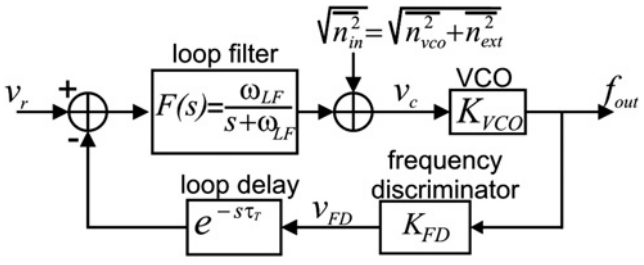

Fig. 1 *FLL architecture*

open-loop transfer function of the FLL is

$$H_{\mathrm{OL}}(s) = K_{\mathrm{FD}} K_{\mathrm{VCO}} \frac{\omega_{\mathrm{LF}}}{s + \omega_{\mathrm{LF}}} \mathrm{e}^{-s\tau_{\mathrm{T}}} \tag{6}$$

The Bode criterion establishes that a feedback system is stable if, in its open-loop frequency response, the phase is greater than $-180°$ when the magnitude crosses over 0 dB. This crossover 0 dB frequency, $\omega_{0\,\mathrm{dB}}$, is

$$\omega_{0\,\mathrm{dB}} = \omega_{\mathrm{LF}} \sqrt{\left(K_{\mathrm{FD}} K_{\mathrm{VCO}}\right)^2 - 1} = \omega_{\mathrm{LF}} \sqrt{G_{\mathrm{OL}}^2 - 1} \tag{7}$$

A well-known rule of thumb developed by Bode advices is that a loop system should have a phase margin greater or equal than 45° [19]. So, at $\omega_{0\,\mathrm{dB}}$, the phase of the open-loop function must be greater than $-135°$. The stability condition is obtained by substituting (7) in the phase response of (6), yielding

$$\omega_{\mathrm{LF}} \tau_{\mathrm{T}} \sqrt{G_{\mathrm{OL}}^2 - 1} + \mathrm{atan}\left(\sqrt{G_{\mathrm{OL}}^2 - 1}\right) \leq \frac{3\pi}{4} \tag{8}$$

For practical situations in which $G_{\mathrm{OL}} \gg 1$, the 'arctangent' term in (8) can be approximated by $\pi/2$. So, the stability criterion is finally obtained as

$$\omega_{\mathrm{FLL}} \simeq \omega_{\mathrm{LF}} G_{\mathrm{OL}} \leq \frac{\pi}{4\tau_{\mathrm{T}}} \tag{9}$$

This equation establishes that the maximum frequency at which the loop is still able to achieve noise reduction is limited by the loop delay τ_{T}.

Numerical simulations of the complete FLL loop, including the non-linear discriminator have indeed confirmed that this stability analysis is correct and that condition (9) has to be fulfilled to keep the loop stable.

As the loop delay is not known in advance, a judicious choice to avoid instability is to set ω_{FLL} as low as possible. From (5), it can be seen that setting $f_{\mathrm{FLL}} = \omega_{\mathrm{FLL}}/2\pi \approx 3$ MHz and $f_{\mathrm{LF}} = \omega_{\mathrm{LF}}/2\pi \approx 300$ kHz gives an ideal FLL noise reduction (at the desired frequency at 1 MHz off the carrier) of approximately 9.8 dB in the ideal noiseless situation $\eta_n = 0$. This demands for a DC open-loop gain $G_{\mathrm{OL}} \approx 9$; so, for the selected VCO with $K_{\mathrm{VCO}} \approx 450$ MHz/V, requires a discriminator's sensitivity $K_{\mathrm{FD}} \approx 20$ V/GHz. From (9), it can be seen that setting this value of ω_{FLL} allows for a maximum delay τ_{T} of 42 ns for the loop electronics, which is a reasonable value easily attainable in practice. Furthermore, this achieves the approximation $\omega_{\mathrm{LF}} \tau_{\mathrm{T}} \ll 1$ made in (5).

3 Delay line FD

3.1 Analysis

The FD is the most critical block of the FLL. To achieve the required wideband performance, a wideband delay line discriminator [20], as shown in Fig. 2, has been proposed. It is composed of two main blocks: (i) a frequency to phase converter that transforms the frequency deviations at the discriminator input (f_{out}) to phase deviations and (ii) a phase detector that generates an output voltage (v_{FD}) proportional to the inputs phase-shift.

The frequency to phase converter comprises a power splitter, a delay line (τ_{d}) and a tunable phase-shifter to

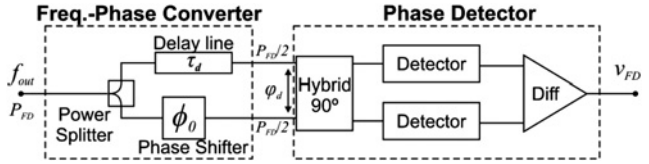

Fig. 2 *Delay line FD architecture*

adjust the discriminator at its quadrature point. The phase detector comprises an ultra-wideband 90° hybrid [18], two diode detectors and a differential amplifier.

The response of the FD can be analysed under a RF sinusoidal excitation. The discriminator's output can be calculated as

$$v_{\mathrm{out}}(t) = K_{\phi} \sin\left(\omega_{\mathrm{out}} \tau_{\mathrm{d}} - \phi_0\right) \tag{10}$$

where K_{ϕ} is the phase detector sensitivity.

As seen in (10), the static response of the FD is a sinusoid with a period $1/\tau_{\mathrm{d}}$. It is important to work in the points where the 'sine' function in (10) crosses over 0, that is, the quadrature points [21]. These points offer two advantages: the FD has the maximum sensitivity and the 'sine' term in (10) can be linearly approximated. The phase shifter (ϕ_0) is adjusted to maintain the phase difference (φ_{d}) at the input of the phase detector in quadrature, that is

$$\varphi_{\mathrm{d}} = \omega_{\mathrm{out}} \tau_{\mathrm{d}} - \phi_0 = \frac{\pi}{2}(2k+1) \quad \text{for } k = 0, 1, 2, \ldots \tag{11}$$

Assuming quadrature, the FD sensitivity becomes

$$K_{\mathrm{FD}} = 2\pi\tau_{\mathrm{d}} K_{\phi} \tag{12}$$

At a quadrature point, the sensitivity of the phase detector, K_{ϕ} (V/rad), depends on the FD input power P_{FD}. For low input power, that is, under square law regime, the phase detector sensitivity depends linearly on P_{FD}, while for higher powers, where the behaviour is close to an envelope detector, the phase detector sensitivity increases linearly with the square root of the input power (P_{FD}).

3.2 Measurements

Using this architecture, a FD has been designed based on a 15 ns coaxial delay line (Labflex290, $\tau_{\mathrm{d}} = 15$ ns), two diode (Avago HSCH-9161) detectors and a low noise differential amplifier based on LMH6622 and LME49990 operational amplifiers. The power splitter is a 3 dB Wilkinson power divider with return loss better than 25 dB in the ultra-wideband (UWB). The 90° hybrid is a high performance hybrid with amplitude and phase imbalance of ±0.5 dB and ±0.7°, respectively, in the complete UWB. More details of this hybrid can be found in [18]. For the sake of simplicity, the phase shifter in Fig. 2 has not been included in the measured prototype, therefore at this moment the FLL can only be operated at fixed quadrature points spaced $\Delta f_{\mathrm{d}} = 1/\tau_{\mathrm{d}} = 66.6$ MHz along the complete band ranging from 5 to 8 GHz. The measured FD static response is depicted in Fig. 3, for an input FD power $P_{\mathrm{FD}} =$ 3.6 dBm, showing the periodicity of the response (66.6 MHz period). As previously seen in (10), a sinusoidal shape is expected. However, the shape is slightly triangular

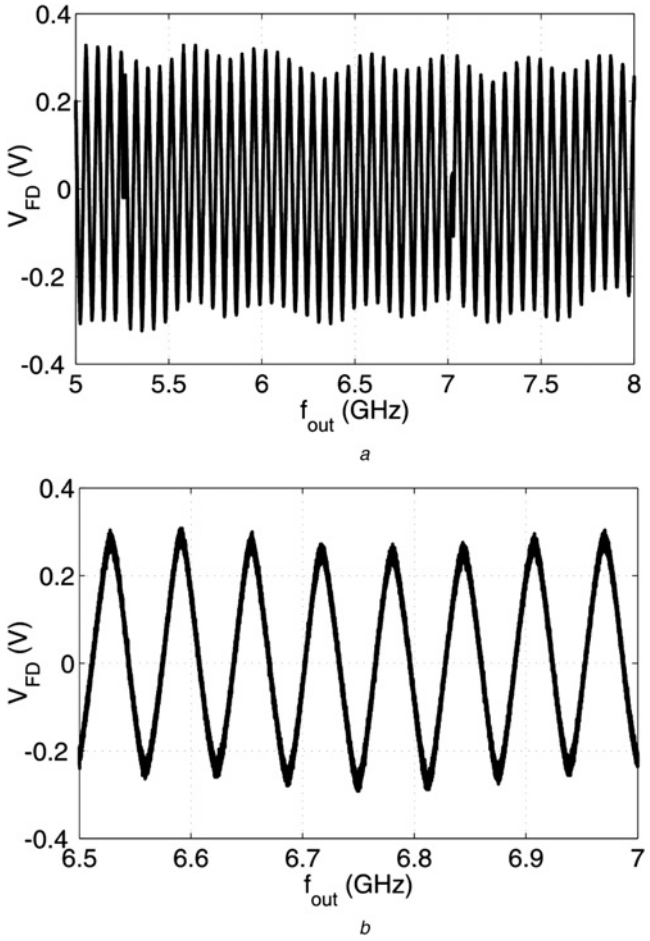

Fig. 3 *FD static response*

a Measured FD static response for a input power $P_{FD} = 3.6$ dBm
b Measurement detail

because the phase detector diodes are not working in square law, but in linear regime. Signal nulls at 5.3 and 7.1 GHz are because of instrument generator switching in the frequency sweep performed.

A more relevant measurement is the FD sensitivity, at the quadrature points, that is, at the frequencies where the prototype static response is 0 V. As seen in Fig. 4, $K_{FD} = 22$ V/GHz up to 8 GHz VCO output frequency, for an input RF power of 3.6 dBm. From (12), the phase detector sensitivity, K_ϕ, can be easily calculated yielding $K_\phi = 0.233$ V/rad.

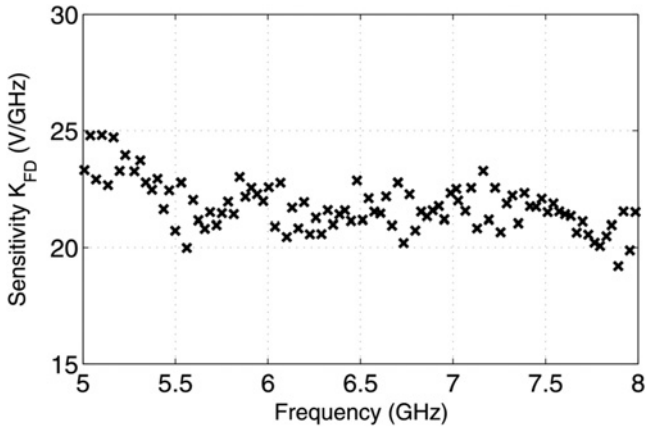

Fig. 4 *Measured FD sensitivity (K_{FD}) in quadrature points*

4 FLL measurement results

A prototype of the FLL has been assembled (Fig. 5*a*) and simulated, including the delay line FD previously described, and a wideband commercial VCO (HITTITE MHC587LC4B) with a maximum sensitivity of 450 MHz/V. In order to connect the VCO output with the FD input, we have used a UWB 10 dB coupler [18]. The direct output of the coupler (with insertion loss lower than 1.35 dB) is connected to the discriminator input while the coupled output (with a coupling level of 10 ± 0.6 dB) is used for phase noise monitoring.

Open-loop response measurements have been performed in order to check the FLL stability. Fig. 6*a* shows measured Bode diagram of the open-loop response at the critical stability point, that is, at the frequency point where the

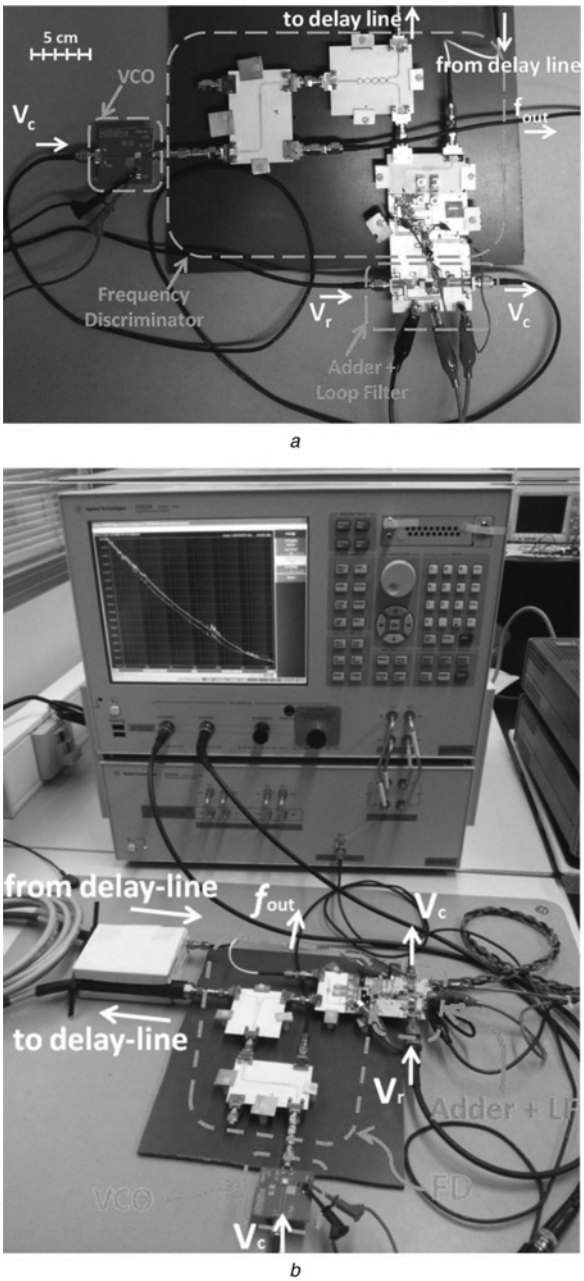

Fig. 5 *Prototype*

a Assembled prototype of the wideband FLL
b FLL Measurement setup

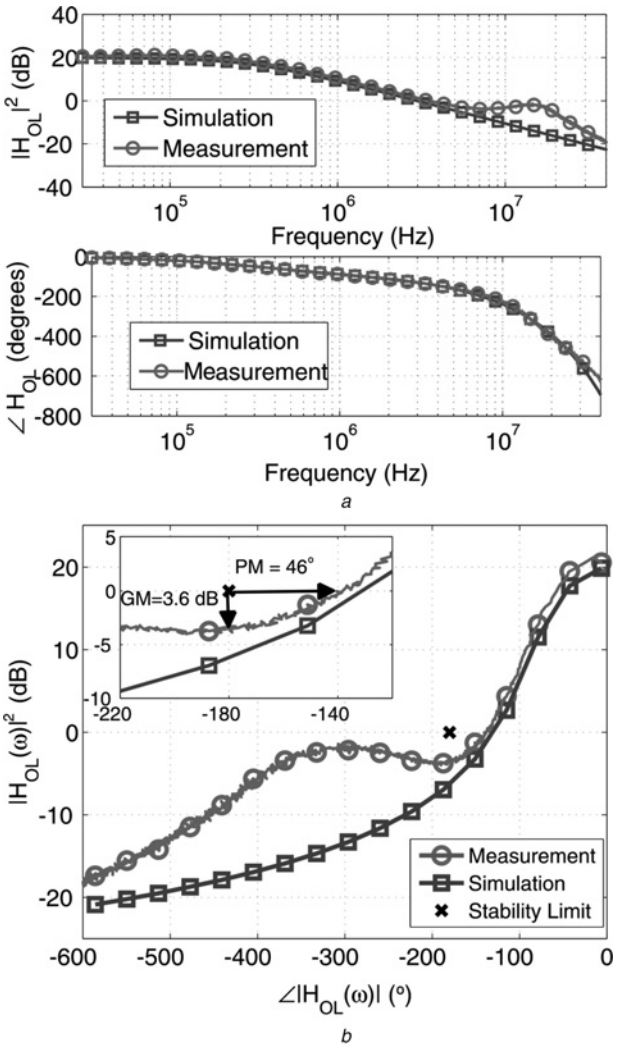

Fig. 6 *FLL open-loop response at 5 GHz*

a Bode diagram
b Magnitude phase diagram

maximum FD sensitivity is obtained (5 GHz). In Fig. 6*b*, the magnitude-phase diagram of the same open-loop response is depicted, where the stability limits of the FLL is more intuitively presented. It is clearly shown that the FLL is stable with a measured minimum phase margin (PM) of 46° and a gain margin (GM) of 3.6 dB. The LF cutoff frequency and open-loop gain obtained yield $f_{LF} = 300$ kHz and $G_{OL} = 20$ dB (10 V/V), respectively.

The mismatch between simulation and measurement observed in Fig. 6 arises because the differential amplifier has been modelled by a first-order model.

Noise characterisation has been carried out with a Signal Source Analyser Agilent E5052B (Fig. 5*b*). First, the phase noise of the free running VCO has been measured and referred to its input through (1). Second, the external noise introduced by FLL circuitry, including the FD, the adder and the LF, has been also characterised. Both results are depicted in Fig. 7*a*. From these measurements, the noise reduction penalty can be easily calculated and is shown in Fig. 7*b*. The maximum noise reduction penalty inside the loop bandwidth is 7 dB.

Finally, the loop has been closed to measure the total FLL phase noise and calculate the achieved noise reduction. Figs. 8 and 9 show a comparison of the measured phase

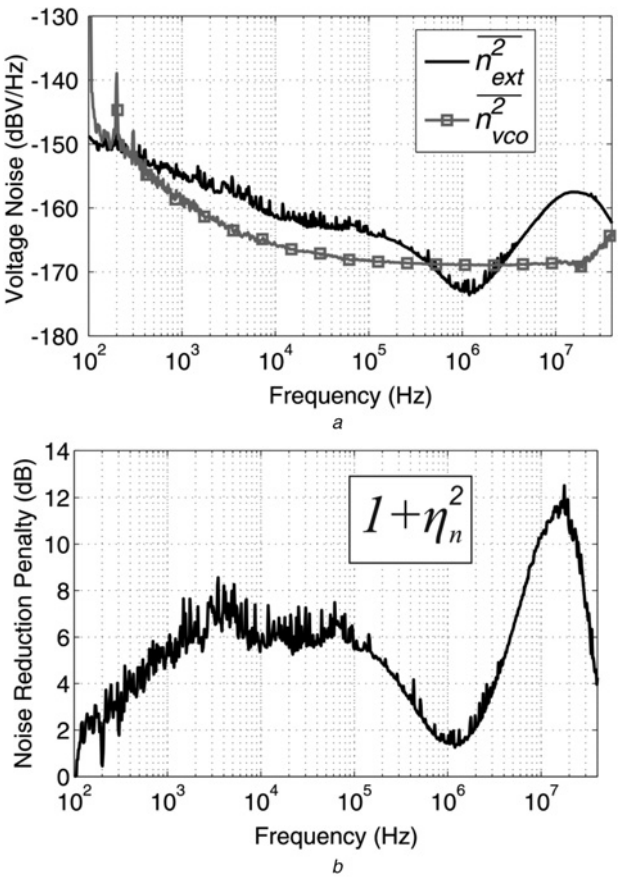

Fig. 7 *Noise characterization*

a Noise voltage referred at VCO input
b Noise reduction penalty $(1 + \eta_n^2)$

noise of the free running VCO (black line), the measured phase noise of the complete FLL (blue line) and the simulated phase noise of the complete FLL (red line), at two different frequency points: 5 and 8 GHz.

The simulation has been obtained by subtracting from the VCO phase noise, the noise reduction predicted by (5) with the measured data: $f_{LF} = 300$ kHz, $f_{FLL} = (1 + G_{OL})) \times f_{LF} =$ 3.3 MHz and noise reduction penalty $(1 + \eta_n^2)$ as plotted in Fig. 7*b*. Good correspondence between simulated and measured results for the complete FLL is observed. Furthermore, a phase noise reduction better than 8–10 dB up to 200 kHz and a reduction greater than 5 dB up to 1 MHz off the carrier has been experimentally measured for

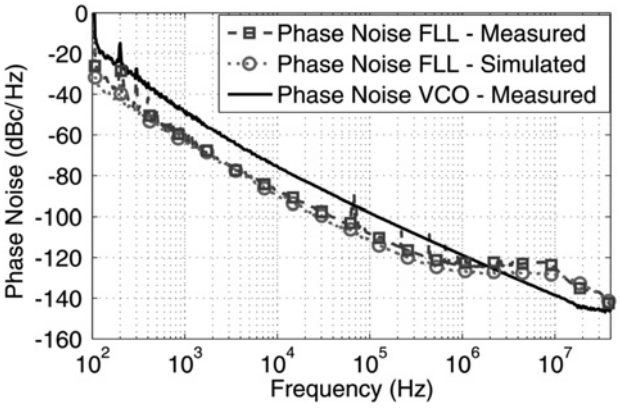

Fig. 8 *FLL and VCO phase noise at 5 GHz*

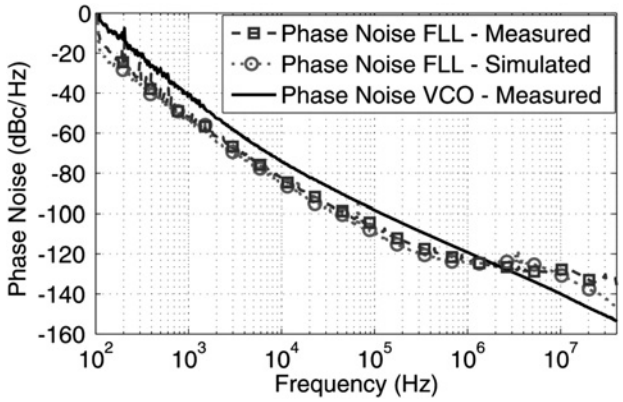

Fig. 9 *FLL and VCO phase noise at 8 GHz*

Table 1 VCOs comparison

VCO	f_0, GHz	FTR, %	Δf, kHz	PN, dBc/Hz	FOM, dBc/Hz
[15]	7.55	30	1000	−115	−202.1
[16]	8.95	16.7	100	−102	−205.5
[17]	5.75	26	100	−98.5	−202
[22]	5.7	8.8	1000	−116	−190
[23]	8.5	12	1000	−108	−188.2
[24]	5	180	1000	−85	−184.1
[25]	11.25	45.3	1000	−87	−181.1
[26]	7.95	15.1	1000	−106	−187.6
HITTITE (MHC587LC4B)	7.5	66.7	100	−95	−212
HITTITE (MHC587LC4B)	7.5	66.7	1000	−119	−213
this work	6.5	46.5	100	−107	−216.5
this work	6.5	46.5	1000	−123.5	−212.5

frequencies between 5 and 8 GHz, yielding to a phase noise of −123.5 dBc/Hz at 1 MHz frequency offset in the entire band.

In order to compare this paper results with the state-of-the-art, low phase noise and wideband VCOs, a well-known figure-of-merit (FOM) has been used [15, 16]

$$\mathrm{FOM} = \mathrm{PN} - 20 \cdot \log\left(\frac{f_0}{\Delta f}\frac{\mathrm{FTR}}{10}\right) \tag{13}$$

where PN is the phase noise at the offset frequency Δf, f_0 is the centre frequency and FTR is the frequency tuning range in percent. The comparison is depicted in Table 1, where we can see that the proposed architecture improves frequency VCOs with other topologies.

5 Conclusions

A FLL architecture that reduces phase noise of a commercial wideband VCO has been presented. Closed equations for the noise reduction and loop stability of this architecture have been derived and used in order to design a FLL. To reach the stringent specifications of the FLL design, a delay line FD with low noise and high sensitivity has been designed and fabricated. FLL measurements yield a phase noise reduction better than 8–10 dB up to 200 kHz and better than 5 dB up to frequencies of 1 MHz off the carrier for frequencies up to 8 GHz for a commercial VCO. In fact, a phase noise better than −107 dBc/Hz at 100 kHz and better than −123.5 dBc/Hz at 1 MHz is obtained, leading to better phase noise results than the state-of-the-art wideband oscillators. Comparison with simulations shows a good agreement, thus assessing the design model and equations. Moreover, this approach could be used in complex microwave synthesiser such as fractional-N PLL to reduce the loop bandwidth, thus simultaneously improving phase noise and spur level performance.

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