Theoretical Consideration on Harmonic Manipulated Amplifiers Based on Experimental Data

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Abstract — This contribution aims at the experimental confirmation of the advantages of the harmonic manipulation theory, using a low-frequency low-cost characterization setup. A 0.5-µm 10x100-µm (1-mm gate periphery) GaN HEMT has been characterized synthesizing at the current-generator plane different load conditions, realizing tuned-load and Class-F operation. The measurements clearly demonstrate the importance of by synthesizing the required loads at the correct reference plane, giving an experimental proof of the performance predicted by theoretical analysis.

Index Terms — FET, harmonic manipulation, integrated circuit measurements, microwave power amplifier, semiconductor device measurements.

I. Introduction

Since the power amplifier (PA) is one of the most critical components in RF and microwave communication systems, a thorough design becomes crucial to optimize its performance and meet the fundamental requirements of high-efficiency operations. In particular, a high absolute value of DC-to-RF efficiency, partly dependent on technological characteristics of the transistor, cannot be reached unless a suitable design methodology is adopted and tailored on the given active device. In this context, the proper manipulation of the harmonic source and load impedances at transistor level gives rise to a clear improvement on PA output power and efficiency [1]. These techniques result in the harmonic manipulation amplifier concept [2],[3].

Several approaches known under the more general name of "waveform engineering" [4], as well as model-based methodologies (e.g., Cripps load-line theory [5]), allow to optimize PA performance by a proper shaping of the voltage and current waveforms at the intrinsic device. However, all these methodologies are based on a simplified description of the transistors, not correctly accounting for nonlinear reactive effects and linear parasitic elements present in the active device. Such phenomena become more pronounced at higher frequencies, preventing the designer from effectively exploiting harmonic manipulation unless an accurate nonlinear transistor model, with access to the intrinsic plane, is available [6].

Approaching the problem from an experimental point of view, for example by using a harmonic load-pull setup, can help to determine the transistor optimum extrinsic loads, at the fundamental and harmonics, which maximize the device performance. Nonetheless, harmonic load-pull setups can be extremely expensive and have the main drawback that raw load-pull data do not allow to consider in depth physical or electrical phenomena inside the transistor, making unfeasible to identify discrepancies between predicted and actual harmonic loading conditions at the current-generator plane.

In this work, by using a low-frequency multi-harmonic load-pull setup [7],[8], harmonic manipulation at the current-generator plane is applied to a GaN transistor, and evaluated in different loading conditions, namely Tuned Load (TL) and Class F [2],[3]. In particular, on the basis of experimental data, we demonstrate the effectiveness of the theoretical approaches and highlight the importance of synthesizing the required harmonic impedances at the correct reference plane. Moreover, the choice of two standard harmonic loading conditions further validates the usefulness of the low-frequency multi-harmonic load pull set-up and its application in the design of PAs.

II. Experimental Results

The measurement system shown in Fig. 1 [7] has been used to fully characterize the behavior of a 0.5-µm 10x100-µm GaN HEMT device from SELEX-ES (Italy). The device was biased at V_{d0} = 22 V and I_{d0} = 50 mA, which corresponds to about 8% of maximum current I_{max} (i.e., 700 mA), thus resulting in a deep Class-AB condition.

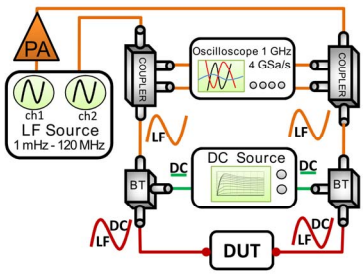

Fig. 1. Measurement system used for the experimental analysis.

The aim is investigating and comparing the electrical performance of the device under two different classes of

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operation exploiting harmonic manipulation, i.e., TL [2] and Class F [3], in order to experimentally verify the theoretical data predicted by simplified models and, at the same time, give a validation of the low-frequency methodology used for tests. The measurement setup is based on multi-harmonic excitations [7],[8]: a $f_0 = 2$ MHz fundamental frequency is conveniently adopted in order to operate above the cut–off of the low-frequency dispersive effects [9], and to neglect the transistor linear and nonlinear reactive phenomena. Such a setup operates as a vector multi-harmonic active load-pull system: by controlling the amplitude of gate and drain incident waveforms and their relative phase, different load terminations can be arbitrarily synthesized at the fundamental and harmonic frequencies for a given bias condition.

It must be emphasized that this setup can directly characterize the intrinsic current generator of an electron device and, as a consequence, its loading conditions. In such a way, one can easily investigate the discrepancies existing between the theoretical and actual loading conditions to be synthesized at the fundamental and harmonic frequencies for every specific class of operation.

The measurement setup is fully controlled via an IEEE488 standard interface by means of NI LabVIEW. We set a grid of impedances at the fundamental frequency and, after properly setting the harmonic terminations to obtain TL and Class-F operation, we carried out measurements for different input power levels. To guarantee safe operating conditions, the setup control software allows to properly set compliances both on the average and instantaneous values of the electrical quantities at the device ports. In particular, the gate and drain average currents under DC and dynamic operation and the maximum values of the incident signals and drain-gate dynamic voltage can be fixed. This is very useful when reliability issues have to be considered. In the presented study we set a maximum drain-gate dynamic voltage value of 50 V.

As a first experiment, we consider the TL operation, setting 2nd and 3rd harmonics to be a short circuit. As shown in Fig. 2, three different impedances (i.e., 43 Ω, 70 Ω and 88.5 Ω) are synthesized at f_0, with the harmonics short circuited. The load lines corresponding to these three terminations are shown in Fig. 3a, at the highest input-power level, whereas in Fig. 3b, drain efficiency as function of output power is shown for all the input power values. As can be noted, by increasing the load impedance, the efficiency increases, whereas the maximum output power decreases due to an earlier saturation of the active device (blue line in Fig. 3a). Among these three conditions, we choose $Z_{L1,TL} = 70\ \Omega$ as the best trade-off, corresponding to the dotted red line in Fig. 3. This is the optimum load resistance calculated at the given Class-AB bias condition [1],[2], for which the transistor reaches a maximum output power of 3.15 W and 69.3% of drain efficiency.

As discussed in [1]-[3], the optimal condition at the fundamental frequency for Class-F operation is $1.15*Z_{L1,TL}$. For this reason, $Z_{L1,F} = 81\ \Omega$ was synthesized at the fundamental frequency, setting the second and third harmonics to be a short and open circuit, respectively (see red circles in Fig. 2). The measured time-domain waveforms of the drain voltage and current for this Class-F operation are reported in Fig. 4, for different input power levels. In this case, a maximum output power of 3.17 W with a drain efficiency higher than 76% were measured.

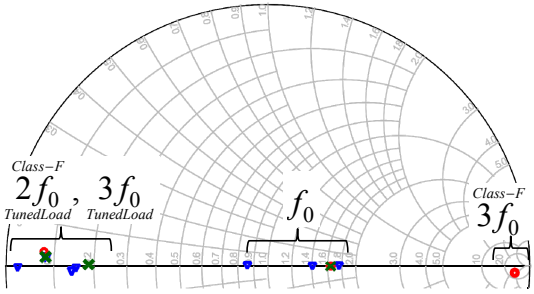

Fig. 2. Load terminations synthesized at fundamental f_0 = 2 MHz and harmonics, $2f_0$ and $3f_0$, on a 0.5-µm 10x100-µm GaN HEMT biased at $V_{d0} = 22$ V, $I_{d0} = 50$ mA. TL (blue triangles and green cross), Class F (red circles).

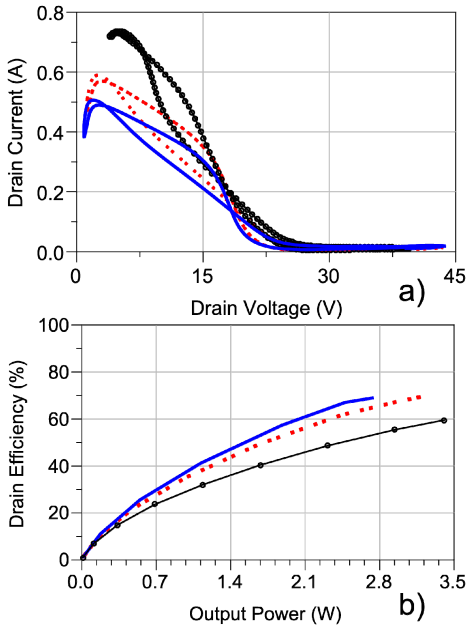

Fig. 3. Load lines (a) and drain efficiency versus output power (b) measured at 2 MHz for the load impedance of 43 Ω (black circles), 70 Ω (red dotted line) and 88.5 Ω (blue solid line) under TL operation (i.e., second and third harmonics are shorted).

The measured voltage waveform shows the theoretical square shaped behavior as expected from a Class-F approach when the 3rd-harmonic component starts to appear. Moreover, both the maximum output power and efficiency are improved, with respect to the TL termination $Z_{L1,TL}$.

Finally, in order to demonstrate that the obtained improvements are due to the proper 3rd-harmonic termination, and are not related to the increased impedance $Z_{L1,F}$ with respect to $Z_{L1,TL}$, the same impedance $Z_{L1,F}$ was also synthesized under TL condition. In this case, we found a

maximum output power limited to 2.8 W with 69% of drain efficiency. Fig. 5a shows the load lines corresponding to the different analyzed classes: TL at $Z_{L1,TL}$ and $Z_{L1,F}$, and Class F at $Z_{L1,F}$. In Fig. 5b, the drain efficiency as a function of the output power is reported in the different classes of operation and for all the characterized input power levels.

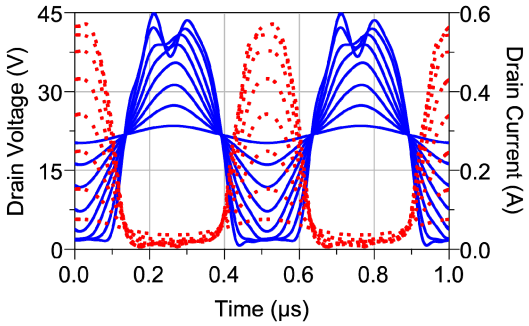

Fig. 4. Time-domain voltages (blue solid lines) and current (red dotted lines) measured under Class-F operation at $Z_{L1,F} = 81\ \Omega$, $2f_0$ shorted and $3f_0$ opened..

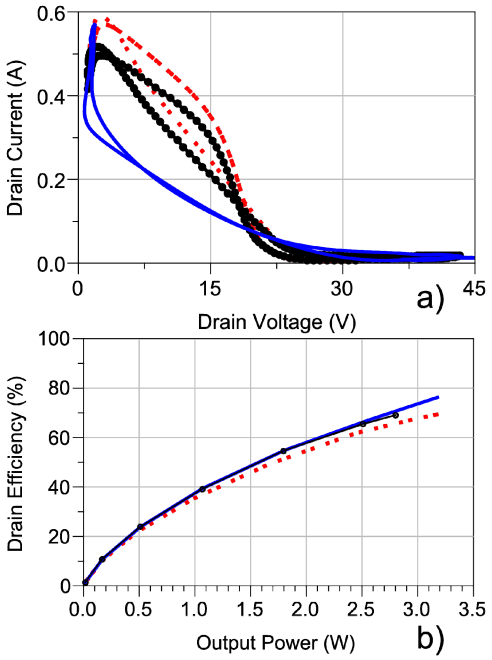

Fig. 5. Load lines (a) and drain efficiency versus output power (b) measured at 2 MHz for the load impedance of 70 Ω ($Z_{L1,TL}$) under TL operation (red dotted line), and 81 Ω ($Z_{L1,F}$) under TL operation (black circles) and Class-F operation (blue solid line).

Fig. 6 shows the time-domain waveforms of the drain voltage and current corresponding to the load lines in Fig. 5a.

The results of the characterization are summarized in Table I in terms of output power and drain efficiency. From the measured data, it can be observed that the proper adoption of a Class-F strategy allows a simultaneous increase of both output power and efficiency levels with respect to the TL condition, as theoretically predicted by simplified models [1].

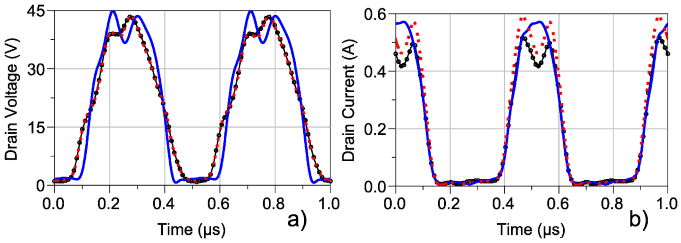

Fig. 6. Time-domain voltages (left) and current (right) measured under TL operation at $Z_{L1,TL}$ (red dotted line) and $Z_{L1,F}$ (black circles) and Class-F operation (blue solid line).

TABLE I
PERFORMANCE OF 0.5-µm 10x100-µm GAN HEMT

	TL @ $Z_{L1,TL}$	**Class F @ $Z_{L1,F}$**	**TL @ $Z_{L1,F}$**
Output Power	3.15 W	3.17 W	2.8 W
Drain efficiency	69.3 %	76.2 %	69 %

III. CONCLUSION

In this paper, an experimental confirmation of the benefit of harmonic manipulation theory has been discussed. Using a low-frequency measurement setup, a 0.5-µm 10x100-µm GaN HEMT has been characterized in three different load conditions at the current-generator plane, showing the effectiveness of the theoretical analyses and the validity of multi-harmonic low-frequency approach.

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